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Im Auftrag

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A current folding cell for an analog-to-digital converter

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A current folding cell for an analog-to-digital converter

Field of the invention

The invention relates to current folding circuit cells. It also relates to an analog-to-digital conversion circuit (A/D conversion circuit) and mixers employing such folding circuit cells. It also relates to signal processors incorporating such A/D conversion circuits, mixers or folding cells.

Description of the prior art

Folding circuit cells have been extensively used to reduce the number of components and hence the cost and power consumption in analog-to-digital converters. As an example, Fig. 1 shows a schematic diagram of a conventional serial type analog-to-digital converter comprising folding circuits I-1...I-5 in cascade. Each folding circuit produces a V-shaped output signal, which is presented to the input of the next folding circuit. Fig. 2a to 2e show the outputs of the folding circuits as a function of the input signal. Each folding block also contains a comparator which provides a digital output indicating the sign of the signal at the input of the folding block. Such a converter needs one folding circuit cell per bit, and therefore only needs a small number of components.

To produce such a continuous V-shaped signal exhibiting two opposite slopes from a single signal, a sign reversal operation for part of the input range or a difference producing circuit is required. Continuous folded output currents exhibiting changing slopes as a function of the input currents can be obtained without sign reversal operations in the folding cell if more than one time-varying current is applied to the current folding cell. Continuous means in this context that the folded current signal does not exhibit abrupt steps, it only changes slope abruptly.

US patent No. 4599602 describes such a conventional serial type A/D converter using folding circuit cells in cascade, where each cell converts a differential potential input into a current difference using a differential

amplifier. A comparator included in the cell switches over the current paths for the differential current to implement the sign reversal and to obtain a folding characteristic. The current difference is further converted into a differential voltage, which serves as output of the folding circuit cell and is applied to the next cell in the cascade.

An example of applying input currents to more than one current input to obtain two different slopes is described in GB patent No. 1266962. One current input receives the input current while the second one receives the input current with the opposite sign. The signals are fully rectified and then transferred to the next stage. The disadvantage of such full rectifier circuit is that when current paths for the signal currents are switched from one current path to another, the current in both paths is zero. This requires operating the non-linear elements at effectively zero current around the switching point. This yields a large input impedance around the switching points requiring large voltage swings around the zero transition. Any capacitance associated with the input nodes has to be charged and discharged by the input current over this large voltage range rendering this circuit slow.

A current folding cell addressing this speed problem in part is described in US patent No. 4179687. The circuit provides two current paths, only one of which is conducting significant current at a given time. The current in one of the two paths is fed to a current sink and not further used. The current in the other path is used for further comparisons. A cascade of N such cells leads to a folded signal with N+1 line segments.

Another such current folding cell is described in US patent No. 4325054. It provides two alternate paths for the input current. The value of the input current determines along which of the two current paths the input current will flow. The currents flowing through these two alternate paths are fed to a difference producing circuit, which in the embodiment described is implemented using a current-to-voltage conversion for the current in each of the two current paths, and a difference producing circuit using the two voltages generated in these current to voltage converters as

input. An alternate implementation for the difference producing circuit is based on taking the difference of the two currents directly, which requires a sign reversal of one of the two currents. Such a sign inversion can be implemented using a current mirror or a circuit using an operational amplifier. An example of this is described in US patent No. 4574270. Without a sign reversal the folding circuit of US patent No. 4325054 still works, but N-1 folding cells are needed to obtain a folding characteristic with N segments, which yields a slow signal and a costly solution in terms of area and power for large values of N.

Voltage-to-current conversion circuits, current-to-voltage conversion circuits, current mirrors, and circuits implementing a current sign reversal are sensitive to device parameters and device parameter mismatch. Device parameter mismatch can be improved by increasing device size but this leads to higher cost and larger capacitive load. If this larger capacitive load is seen by the varying signal a slower circuit is obtained.

Folding circuit cells which include voltage-to-current or current-to-voltage conversion circuits acting on the time-varying signal, or which include current mirrors or current sign reversal circuits in the path of the time-varying signal, therefore limit the speed and/or the accuracy of the serial analog-to-digital converter in which they are used.

Sometimes switches are used to switch from one current path to another and this is controlled by some controlling input, i.e. the differential voltage on the gates of a differential transistor pair. These switches often are the cause of large switching transients in the signal current, or they require complicated circuitry to minimize this effect. In addition, a large voltage swing is often required to control the switches. If this large swing is to be applied at high frequency, a power penalty is incurred.

In the prior art, all folding circuits with current inputs and current outputs which can be cascaded without any intermediate circuitry to produce a continuous folded signal at the output with 2N segments where N is the number of stages satisfy at least one of the following conditions:

- The folding cell contains a current sign reversal operation on the time-varying signal (like a current mirror for instance);

- The folding cell contains a current difference operation which requires a current sign reversal operation on the time-varying signal;

- The folding cell requires a current-to-voltage conversion operation on the time-varying signal and later on a voltage-to-current conversion;

- The folding cell requires comparatively large voltage transitions around at least some of the switching points, because the currents through some of the various current paths provided for each input signal are substantially zero when current paths are switched from one to another for that input signal.

In contrast, the folding circuits presented here can be cascaded to construct an analog-to-digital converter without the need for a sign reversal, or voltage-to-current or current-to-voltage conversion, and provide the possibility of obtaining a folding characteristic with 2 to the power N segments with only N folding circuit cells, and this without requiring that currents through the various current paths provided for the different input signals are substantially zero when current paths are switched from one to another. Due to the small number of components required even for a large number of segments in the folding characteristic, these folding circuits therefore present a low cost and low power solution for the same performance. In addition, due to the limited sensitivity to mismatch of the components in the path of the time-varying signal, those components can be made small, thus yielding lower parasitic capacitances and higher speed. The higher speed is further enhanced by the fact that signal current is transferred from one current path to another without requiring substantially zero current in at least one of the current paths near the switching point. Furthermore, the limited number of components allows to actively compensate some fraction of these parasitic capacitances, the small number of components allowing this without a large power

penalty. The invention described here also includes some ways to compensate for parasitic capacitances.

Several techniques have been proposed to reduce or eliminate cell mismatches in analog-to-digital conversion to improve the linearity of the conversion. One example is the use of chopper amplifiers and filtering in the digital domain. Such a technique usually introduces considerable additional power and circuit complexity.

US patent 5,835,048 and 6,014,098 describe a way to reduce cell mismatches in a plurality of cells containing a differential amplifier having first and second branches. The technique uses averaging impedances, preferably resistors, connected between the output terminals in the first branches of the differential amplifier, and the output terminals in the second branches of the differential amplifier, in successive pairs of cells. The impedances have relatively low values, particularly compared to the impedances of current sources connected to the branch output terminals. While this method provides for significant improvement compared to its prior art in terms of linearity improvement of the converter, the current folding cell introduced here allows for an even further improvement. This is due to the fact that there exists a well defined relationship between the output currents of a folder constructed from a cascade of such current folding cells described here. Instead of only reducing the influence of offsets due to averaging, our technique provides the possibility of fully eliminating some offset contributions, and this with only a small number of components. Since our technique allows to fully eliminate offset contributions from some components, these components can be designed with smaller dimensions. This results in a smaller circuit and hence a reduced cost, and also yields a speed advantage as the parasitic capacitances associated with these components is reduced.

Testing of analog-to-digital converters is often time consuming and often requires special equipment, both of which cause the testing to be important in the overall cost of such converters. The folding cells described here can provide two digital outputs per cell or 2N digital signals

for an N bit converter. This redundancy can be used advantageously to simplify the testing and significantly reduce the testing cost for a converter based on these folding cells.

Mixers are often used in systems for telecommunication and networks to superimpose and extract a signal from the carrier. Very often an analog-to-digital converter is required after the mixer. The folding cells described here allow to implement a mixer, and therefore allow to implement a mixer-converter combination where no signal conversion (e.g. current-to-voltage) is required eliminating conversion errors, and where several biases could be shared yielding a smaller circuit area, lower power, and hence a reduced circuit cost.

Summary of the invention

Folding circuit cells which include voltage-to-current or current-to-voltage conversion circuits acting on the time-varying signal, or which include current mirrors or current sign reversal circuits in the path of the time-varying signal, limit the speed and/or the accuracy of the circuit in which they are used.

Because the currents through some of the various current paths provided for the different input signals are substantially zero when current paths are switched from one to another, folding cells which require comparatively large voltage transitions around at least some of the switching points are limited in speed.

Continuous folded output currents exhibiting changing slopes as a function of the input currents can be obtained without sign reversal operations in the folding cell if more than one time-varying current is applied to the current folding cell. Continuous means in this context that the folded current signal does not exhibit abrupt steps, it only changes slope abruptly. Abrupt steps can be created by current switches, but such current switches can introduce significant switching noise in a circuit and can cause significant speed limitations.

An object of the present invention is therefore a current folding circuit cell where:

- currents at a plurality of current inputs are transferred to a plurality of current outputs via different current paths,

- the magnitude or sign of the current signals only determines which current path is taken by each current,

- signal currents change from one current path to another without requiring substantially zero current in at least one of the current paths,

- currents are only added and not subtracted.

It is a further object of the invention that this cell can comprise:

At least two current input terminals;

At least two current output terminals;

A current summing circuit at every current input terminal where more than one input current arrives yielding a single input current at every current input terminal, where the single input current is time-varying, and proportional to a signal to be folded, for at least one of the current input terminals;

A circuit providing at least two alternate current paths for the input current associated with at least one of the input terminals, the sign or magnitude of these input currents determining the current path taken to conduct each of the input currents;

A current summing circuit at every current output where more than one current arrives yielding a single output current at every current output;

In principle, adding currents can be done by providing wires to connect the output terminals providing these currents together and further providing a wire to the input terminal for the current sum. In practice, currents might be added using a more complicated way to avoid a large capacitive load at the input. For instance, some currents can be added on one node, different from the node sensitive to the parasitics, and the result can be transferred to the sensitive node using a cascode transistor which does not represent a large capacitive load on this sensitive node.

It is a further object of the invention that in this folding cell at least two alternate current paths for the input current are provided for the input current associated with at least two of the current input terminals.

It is a further object of the invention that this folding cell can comprise:

Two current input terminals and two current output terminals;

A current summing circuit at every current input terminal where more than one input current arrives yielding a single input current at every current input terminal, a first input current for the first current input terminal and a second input current for the second current input terminal, both input currents being time-varying and proportional to a signal to be folded;

A circuit providing two alternate current paths for the first input current, the sign of which determines the current path taken to conduct this first input current, and further providing two alternate current paths for the second input current, the sign of which determines the current path taken to conduct this second input current;

A current summing circuit to add the current from one of the current paths associated with the first current input to one of the current paths associated with the second current input, and including a means to

provide the result of the addition to the first current output of the folding circuit cell;

A current summing circuit to add the current from one of the current paths associated with the second current input to one of the current paths associated with the second current input, and including a means to provide the result of the addition to the second current output of the folding circuit cell;

A further object of the invention is that at the first current input terminal a first input current can be added to a first reference current provided by a first reference source, and at the second input a second input current can be added to a second reference current provided by a second reference source. Please note that the reference currents can be generated as a sum of several reference currents.

A further object of this invention is that a comparison means can be included in the current folding cell yielding a digital output determining the sign or whether the current is above or below a certain threshold for the input current associated with at least one of the current input terminals, or that a comparison means can be included in the folding cell to determine which of two input currents each associated with a different current input terminal is larger.

It is a further object of the invention that for such folding cells with two current input terminals the input current at the first input terminal can be made equal in magnitude and opposite in sign to the input current at the second input terminal. This provides an easy way to cascade these current folding circuit cells without any intermediate circuit to construct an analog-to-digital converter to produce a folded signal at the output with 2N segments where N is the number of stages in the cascade. Using this approach, a digital code with Gray-code properties is obtained with only one folding cell per bit in the cascade. The need for only one cell per bit yields a very small number of components resulting in a low power

and low cost solution. This will be further detailed in the discussion on the preferred embodiments.

It is therefore a further object of the invention that these current folding circuit cells can be used in an analog-to-digital converter.

In addition it is therefore a further object of the invention that a cascade of these current folding circuit cells can be used in such a converter, wherein the output terminals of a preceding stage cell are connected to the inputs of a succeeding stage cell.

It is a further object of the invention that the outputs of these folding cells can be combined by for instance adding them, before inputting them to a succeeding stage cell. This can be advantageous for instance to increase the operating speed of the analog-to-digital converter or to increase the size of the input signal of the succeeding cell.

It is a further object of the invention that gain stages can be inserted in-between consecutive stages of folding cells. This will provide an increase in conversion speed for the following stages for the same number of stages.

It is a further object of the invention that an analog-to-digital converter can be constructed from a plurality of cascades of such current folding cells, where the inputs of the first cells of the different cascades have some relation with respect to one another.

It is a further object of the invention that this relation can comprise a constant offset between the inputs of the different cascades.

It is a further object of the invention that this relation can comprise an offset which is well defined between the zero transitions, but which varies with the input signals.

It is a further object of the invention that due to the well-defined relationship between the output signals of these folders, they can be combined or mutually compared to provide signals which can be fed back to the circuitry providing the current inputs to these folders. Such feedback loops can be used to reduce or eliminate mismatch between components or to reduce or eliminate common mode components in input signals.

It is a further object of the invention that a sample-and-hold or track-and-hold circuit can be placed in front of such folding cells or cascade of folding cells, or in-between consecutive stages of folding cells to improve the conversion rate of the circuit.

Testing integrated circuits often forms an important factor in the overall cost of these circuits. The folding cell can be provided with one comparison means per current input terminal. In case there is a relationship between the currents at the different current input terminals, some degree of redundancy is created which can be beneficially used for testing.

A testing method is therefore a further object of the invention where the digital outputs of the comparison means in the folding cell are mutually compared to detect anomalies in the operation of the current folding circuit cell.

Note: the following might be regarded as a separate invention.

It is a further object of the invention that the capacitive loading seen by a current in a node of a circuit which transfers the current or part thereof from one or more current inputs to one or more current outputs can be minimized by means of a shield driven by a circuit following the ac component of this one node. Doing so can yield an increase in circuit speed.

It is a further object of the invention that the capacitive loading seen by a current in a node of a circuit which transfers the current or part thereof from one or more current inputs to one or more current outputs can be compensated for by re-injecting a fraction or the totality of the

capacitive current, or an approximation thereof, with the opposite sign into said node. Doing so can yield an increase in circuit speed.

Brief description of the drawings

The invention and its additional features, which may optionally be used to implement the invention to best advantage, will be apparent from and elucidated with reference to the embodiments described hereafter with reference to the accompanying drawings, wherein:

Fig. 1 shows, in block diagram form, how a prior art serial analog-to-digital converter is constructed from a cascade of folding circuit cells. In the figure the cascade comprises 5 folding circuit cells;

Fig. 2a to 2e refer to Fig. 1 and show the signal shape of the output of folding circuit cell I1 to I5, respectively, as a function of the input signal of the prior art converter shown in Fig. 1;

Fig. 3 shows an embodiment C1 of one half of the current folding cell and a possible schematic B1 to bias the circuit C1;

Fig. 4 shows an embodiment C2 of one half of a current folding cell including a comparison means to determine the sign of the sum of the currents at the input, and a possible schematic B2 to bias the circuit C2;

Fig. 5 shows a block diagram representation of the circuit C2 of Fig. 4;

Fig. 6a and 6b show the output currents $I_{out}u$ and $I_{out}d$ of the circuit C1 of Fig. 3, and of the circuit C2 of Fig. 4 as a function of the input current. The sign of the current is positive if it flows in the direction of the arrow;

Fig. 7 shows an implementation example of the novel folding circuit cell comprising two circuits C2 from Fig. 5;

Fig. 8 shows an implementation example of the novel folding circuit cell comprising two circuits C2 from Fig. 4, where at each current input a signal current and a reference current are summed;

Fig. 9 shows the circuit of Fig. 8 in more detail;

Fig. 10 shows a block diagram view of the novel folding circuit cell of Fig. 8;

Fig. 11 shows, for the folding circuit cell of Fig. 8, the sum of the current outputs $I_{out}u1$ and $I_{out}u2$ as a function of I1 in the folding circuit cell, and this for the case where I1 is equal to I2, but opposite in sign. The resulting current is the current output $I_{out}2$ of the folding circuit cell;

Fig. 12 shows, for the folding circuit cell of Fig. 8, the sum of the current outputs $I_{out}d1$ and $I_{out}d2$ as a function of I1 in the folding circuit cell, and this for the case where I1 is equal to I2, but opposite in sign. The resulting current is the current output $I_{out}1$ of the folding circuit cell;

Fig. 13 shows, in block diagram form, how a novel serial analog-to-digital converter is constructed from a cascade of novel current folding circuit cells. In the figure, the cascade comprises n cells;

Fig. 14 shows I1 of the second folding circuit cell in the cascade of Fig. 12 as a function of I1 in the first cell, for the case where I1 in the first cell is equal to I2 in the first cell, but opposite in sign;

Fig. 15 shows I2 of the second folding circuit cell in the cascade of Fig. 12 as a function of I1 in the first cell, for the case where I1 in the first cell is equal to I2 in the first cell, but opposite in sign;

Fig. 16 shows I1 of the third folding circuit cell in the cascade of Fig. 12 as a function of I1 in the first cell, for the case where I1 in the first cell is equal to I2 in the first cell, but opposite in sign;

Fig. 17 shows I2 of the third folding circuit cell in the cascade of Fig. 12 as a function of I1 in the first cell, for the case where I1 in the first cell is equal to I2 in the first cell, but opposite in sign.

Fig. 18 shows in more detail how a cascade of current folding cells of Fig. 8 can be constructed for use in an analog-to-digital converter;

Fig. 19 shows the core of another embodiment of the current folding cell;

Fig. 20 shows the core of another embodiment of the current folding cell;

Fig. 21 shows the core of another embodiment of the current folding cell;

Fig. 22 shows the core of another embodiment of the current folding cell;

Fig. 23 shows a possible way of how the proper bias can be provided for the core of the current folding cell shown in Fig. 19;

Fig. 24 shows a possible way of how the proper bias can be provided for the core of the current folding cell shown in Fig. 20;

Fig. 25 shows an alternative way to apply the proper bias to the core of the current folding cell shown in Fig. 20;

Fig. 26 shows an embodiment of the current folding cell based on the core shown in Fig. 19, where at each of the two inputs of the current folding cell the input current is added to one reference current, and where the means for proper biasing of the core is provided;

Fig. 27 shows how the means for proper biasing of the core of a previous current folding cell can be provided by the succeeding current folding cell in a cascade of current folding cells;

Fig. 28 shows in more detail how a cascade of current folding cells containing the core of Fig. 19 can be constructed for use in an analog-to-digital converter;

Fig. 29 gives a block diagram representation of the circuit in Fig. 21;

Fig. 30 gives a block diagram representation of another cascade of folding circuit cells;

Fig. 31 gives a block diagram representation of the cascade of folding circuit cells of Fig. 30;

Fig. 32 illustrates how several cascades of folding circuit cells can be put in parallel for the construction of an analog-to-digital converter;

Fig. 33 shows the magnitude of the output currents after the first stage in the cascades of Fig. 32;

Fig. 34 shows the magnitude of the output currents after the second stage in the cascades of Fig. 32;

Fig. 35 shows the magnitude of the output currents after the third stage in the cascades of Fig. 32;

Fig. 36 shows the magnitude of the output currents after the fourth stage in the cascades of Fig. 32;

Fig. 37 shows the current outputs after addition of the current sources after the fourth stage in Fig. 32;

Fig. 38 illustrates how averaging for the most significant bits can be implemented in case a plurality of parallel folding cells or cascades of folding cells are used in the analog-to-digital converter;

Fig. 39 illustrates one example of how current outputs of an embodiment of the novel current folding cell can be combined;

Fig. 40 shows an example with two folding circuits fed by two differential pairs to explain how offset between the two differential pairs can be reduced or eliminated;

Fig. 41 shows the output currents f1, f1-, f2 and f2- of the two folding circuits of Fig. 40 as a function of the input current, in case no offset is present apart from the one deliberately introduced. The figure also shows a corrective signal "Corr" derived from these output currents which is proportional to the random offset between the two differential pairs shown in Fig. 40;

Fig. 42 shows the output currents f1, f1-, f2 and f2- of the two folding circuits of Fig.40 and the corrective signal "Corr" derived from these output currents, as a function of the input current, in case some random offset is present apart from the one deliberately introduced between the differential pairs shown in Fig. 40;

Fig. 43 shows how the corrective signal "Corr" can be derived from the folder output currents of the circuit shown in Fig. 40. The potential difference between u and v is a measure of the corrective signal "Corr";

Fig. 44 shows how the feedback to correct the offset between the two differential pairs shown in Fig. 40 can be applied in practice, using the signals u and v shown in Fig. 43;

Fig. 45 shows how the input current can be sampled onto the differential pairs of Fig. 40;

Fig. 46 shows another example of how feedback can be used to cancel offset between differential pairs in an analog-to-digital converter;

Fig. 47 further details a possible way to implement the feedback schematically depicted in Fig. 46;

Fig. 48 shows one example of how gain can be applied in between consecutive stages of a cascade of current folding cells;

Fig. 49 gives an example of how one of the output currents of the novel current folding cell can be used for determination of the least significant bits by means of a flash converter;

Fig. 50 illustrates one example of how a current mode mixer based on the novel current folding cell;

Fig. 51 shows a prior art schematic used to limit the influence of the parasitic capacitance C_{par} on the node X1;

Fig. 52 shows an embodiment of a novel arrangement to limit the influence of the parasitic capacitance C_{par} on the node X1;

Fig. 53 shows an embodiment of a different novel arrangement for a current processing circuit to limit the influence of the parasitic capacitance C_{par} on the node X1;

Fig. 54 shows another embodiment of such arrangement for a current processing circuit to limit the influence of the parasitic capacitance C_{par} on the node X1;

Fig. 55 shows another embodiment of such arrangement for a current processing circuit to limit the influence of the parasitic capacitance C_{par} on the node X1.

Description of the preferred embodiments

Fig. 3 shows a prior art circuit C1 which provides two alternate current paths for the input current, and a possible schematic B1 to bias the circuit C1. The circuit operates as follows: a positive current I_{in} injected into the input will cause the voltage of the input to rise above V_{refin}. A negative current I_{in} injected into the input will cause the voltage of the comparator input to fall below V_{refin}. An input current significantly larger than IDC will be absorbed by only one of the two transistors in the circuit C1, the sign of the input current determining by which of the two transistors it will be absorbed. The voltage swing of the input of the circuit C1 will be sufficiently large to be detected by a voltage comparison circuit. Fig. 4 shows the circuit C2 which comprises a circuit C1 and a voltage comparator. A possible biasing circuit B2 is also added. Fig. 5 shows a block diagram view of the circuit C2. The sign of all currents is positive if the direction of the current flow is in the direction of the arrow. Fig. 6a and 6b show the output currents $I_{out}u$ and $I_{out}d$ of the circuit C1, identical for the circuit C2, as a function of the input current, for a bias current IDC sufficiently small compared to the range of the input current to only have one transistor conduct at a given time. The figure confirms that only one of the two current branches conducts at a given time. For a larger IDC the corners in the $I_{out}u$ and $I_{out}d$ signals will be more rounded, current will flow through both transistors at the same time even for a zero input current, and a small non-zero input current will be divided over both current paths.

In the prior art (US patent No. 4179687) the drain of one of the current absorbing transistors was connected to a current sink, and IDC was kept sufficiently small to have only one of the two transistors conduct current at the same time. Here we would like to combine two circuits C1 or C2 and both their current outputs in a special way to provide a circuit with two inputs and two outputs. Fig. 7 shows an implementation example of the novel folding circuit cell comprising two circuits C2 of Fig. 4 and a means to add several currents IL1...ILn at the first current input, and a means to add several currents IR1...IRn at the second current input, and a means to add the outputs of the two circuits C2. Adding currents is easy, and can be done in principle by connecting the wires that conduct the different currents IL1...ILn and connecting them to the wire which has to

conduct the current I1. The addition of the currents IR1...IRn can be done in a similar way to yield the current I2.

In practice, currents might be added using a more complicated way to avoid a large capacitive load at the input. For instance, some currents can be added on one node, different from the node sensitive to the parasitics, and the result can be transferred to the sensitive node using a cascode transistor which does not represent a large capacitive load on this sensitive node.

Fig. 8 shows an embodiment for the folding circuit cell of Fig. 7, where the currents are added by simply connecting the wires, and where apart from the time-varying input current one reference current is applied to each of both input terminals. Fig. 9 shows the same circuit in more detail, i.e. with the four transistors in the core of the current folding cell, and the comparators. Fig. 10 shows a block diagram form of this new current folding cell. Note that $V_{refin}1$ and $V_{refin}2$ can be different, which would cause the gate biases u1 and u2 to differ and the gate biases d1 and d2 to differ. As explained below this can be required for proper operation of the circuit when this cell is cascaded.

Fig 11 shows for the current folding cell of Fig. 8 the sum of the first output current $I_{out}u1$ of the first circuit C1 or C2 and of the first output current $I_{out}u2$ of the second circuit C1 or C2 as a function of I1 in the folding circuit cell, and this for the case where I1 is equal to I2, but opposite in sign. The resulting current is the current output $I_{out}2$ of the folding circuit cell. Fig. 12 shows for the folding circuit cell of Fig. 8, the sum of the second output current $I_{out}d1$ of the first circuit C1 or C2 and of the second current $I_{out}d2$ of the second circuit C1 or C2 as a function of I1 in the folding circuit cell, and this for the case where I1 is equal to I2, but opposite in sign. The resulting current is the current output $I_{out}1$ of the folding circuit cell. Comparison of Fig. 11 and Fig. 12 shows that for the case where I1 is equal to I2, $I_{out}1$ and $I_{out}2$ are equal in magnitude but opposite in sign. This can be used advantageously when a cascade of such folding cells is used, as shown in Fig. 13. In the figure it is shown how the cascade of current folding cells

is formed by connecting the first output of a preceding stage to the first input of a succeeding cell in the cascade, and by connecting the second output of a preceding cell to the second input of a succeeding cell in the cascade, and this without any intermediate circuitry. In such a cascade of current folding cells it is easy to maintain the condition that I1 is equal to I2, but opposite in sign also for the next cell, and therefore for all cells. To satisfy this the reference currents shown in Fig. 8 need to be equal in magnitude and opposite in sign for the next cell in the cascade. If in addition the magnitude is chosen at half the input range, I1 and I2 of the next cell in the cascade are not only equal in magnitude and opposite in sign, but the zero transition, which corresponds to the point where that next cell will fold the input signal, is centred over the full range. This is illustrated by Fig. 14 and Fig. 15 showing I1 and I2 for the next cell in the cascade. The same can be done for the third cell in the cascade to obtain I1 and I2 in that cell shown in Fig. 16 and 17. Note that the range of the time-varying signal is halved after every stage in the cascade.

This procedure can be repeated for more cells, and one obtains 2^N segments for N current folding circuit cells in the cascade. The comparator outputs of the current folding cells in the cascade will provide the bits determining the value of the input current, the first stage will provide the most significant bits, and the succeeding stages the succeeding less significant bits.

Fig. 18 shows an embodiment of a cascade of four current folding circuit cells in more detail. Such a cascade would be used to construct a four bit analog-to-digital converter. In this figure the comparators are omitted for simplicity. The range for the input current is $[-2^3*I_{lsb}, +2^3*I_{lsb}]$. First consider the case where δ in the figure is equal to zero. The first stage which receives I_{in} and $-I_{in}$ at its inputs will determine the sign of the input currents I_{in} and $-I_{in}$ and does not add any reference current to the input currents at the input. The sign of the two input currents corresponds to the most significant bit and its complement. The first stage provides its output currents (plotted in Fig. 11 and 12) to the inputs of the next stage which adds $4*I_{lsb}$ with the correct sign to these currents and then determines the

sign of the two sums. The sign of these current sums corresponds to the second most significant bit and its complement. The output currents of the second stage are provided to the next stage, which adds $2*I_{lsb}$ with the correct sign to these input currents and then determines the sign of the two current sums. The sign of these two currents corresponds to the third most significant bit and its complement. The last stage finally receives the two output currents of the previous stage at its input and then adds Ilsb (consider δ to be zero first) with the correct sign to each of those currents and determines the sign of these currents to determine the least significant bit.

For the circuit to operate correctly, the reference voltages for the different stages cannot be equal as that would lead to simultaneous conduction of elements which are not supposed to conduct at the same time. For instance, for the maximum positive input current, the output node $I_{out}2$ will be pulled down by the current $-I_{in}$ at the right input of the first cell in the cascade. The left input node of this first stage will be pulled up by the current I_{in}. All this will result in a forward biasing of the NMOS transistor at the upper left of the first stage, while it was intended to be in cut-off for this particular input. This problem is solved by sufficiently increasing the reference voltage (V_{refin} in Fig. 3 or 4) from stage to stage for the left input of the current folding cells, and decreasing the reference voltage from stage to stage for the right input of the current folding cells. This is an example where the reference voltages for the left and the right input of one stage have to be chosen to be different.

Provided this condition is satisfied, the circuit operates as described above: the input currents I_{in} and $-I_{in}$ are transformed into folded signals with two segments after the first stage, four segments after the second stage, eight segments after the third stage, and sixteen segments after the fourth stage. If δ equals zero, the distance between subsequent folding points of the folded signal is 1 I_{lsb}, the first folding point occurring for I_{in} equal to $-7I_{lsb}$ and the last one for I_{in} equal to $+7I_{lsb}$. If comparators are included to detect which of the current paths was taken by I_{in} and its

complement, a digital Gray code is produced corresponding to the input current I_{in}.

It is beneficial to choose δ different from zero to provide two folding points for the output signals of the last stage at different locations within the $2*I_{lsb}$ input range for that stage. This provides additional information on where within this interval the input is located, and can also serve to eliminate sensitivity to errors caused by metastability or slow switching of the folding cell. This is an example of the utility of a folding cell where I1 and I2 of Fig. 7 are not equal in magnitude and opposite in sign.

For a large number of stages in the cascade it might be that the power supply voltage is not sufficiently high to allow the necessary spacing in reference voltages for the consecutive stages without any intermediate circuitry. In that case a folded cascode stage can be inserted in between two particular stages in the cascade wherever necessary. Fig. 23 gives an example of such folded cascode stages for the case that the core of the current folding cell does not consist of four transistors, but of four non-linear elements like diodes. Usually one will choose to use a folded cascode stage both in between the first output of the previous stage and the first input of the succeeding stage, and in-between the second output of the previous stage and the second input of the succeeding stage. In principle one could only insert the folded cascode stage for one of the two signal paths in between two particular stages, and insert a folded cascode stage for the other signal path in between two other stages if necessary.

Fig. 19 through 22 show other examples of embodiments of the core of the new current folding cell. Note that biasing means for these cores are not shown in the figure. All of the cores consist of four circuit elements, each of which provides a signal path from one input towards one of the two outputs. For each of the two inputs we have a signal path towards one of the two outputs and a signal path towards the other of the two outputs. The two signal paths corresponding to each of the outputs are connected together to add the current in the two signal paths. In the

embodiment previously mentioned, a transistor was used in each of the four signal paths. In Fig. 19 the core consists of four non-linear elements, like diodes or diode-connected transistors for instance. Fig. 20, 21, and 22 each use two non-linear elements and two transistors. The cells all operate in the same way. When the input current applied at one of the two inputs changes sign, it is gradually transferred from one current branch to another. Around the zero transition, the current through the current absorbing elements should be well controlled. For the current folding cell of Fig. 8, 9 and 10, it was already explained that this could be done using the biasing circuit B1 in Fig. 3. The cores of the current folding cell shown in Fig. 19 to 22 make use of non-linear elements like diodes, and there a different biasing means needs to be provided. An example for biasing the core of Fig. 19 is shown in Fig. 23: two folded cascode stages are used, each for one output. First consider the case where Il and Ir are equal to zero. The first output of the core is linked to the source of the first cascode transistor, and the second output to the second cascode transistor. The zero input current to the current folding cell can be well defined by adjusting the current through the cascodes and the gate bias of the cascodes. The cascode transistor bias current is cancelled by adding it with the opposite sign to the output current. In case a reference current has to be added at the input of the next cell, it can be included in the biasing current of the cascodes. This way that current which normally has to flow anyway serves to increase the bandwidth of the cascode. This shows an example of the utility of choosing Il and Ir different from zero.

Cascode stages can also be used to provide the bias for the core cells of Fig. 20 through 22. Fig. 24 illustrates this for the core of the current folding cell shown in Fig. 20. However, the gate bias of the two transistors in the core provides already one terminal to control the zero input current of the core. Therefore only one cascode stage with well-defined gate and current bias is necessary to control the zero-input current of the current folding cell. This is illustrated in Fig. 25.

Including also the current references and current summing nodes at the input in addition to the core and its biasing means completes the current folding cell for the core of Fig. 19. This is illustrated in Fig. 26.

The cores of the current folding cell shown in Fig. 19 through 22 are given as an example only. It should be obvious that one could choose combinations of three transistors and one non-linear element as well. In addition, one could replace one or more elements by a full circuit which provides a current path corresponding to each of the elements the circuit is replacing. Such a circuit could contain cascodes, or amplifiers, configured for instance in a feedback loop to increase the output impedance of those cascodes.

The cascodes are not necessary if the input stage of the next cell allows to well define the potential of its input node. An example of this is shown in Fig. 27, where the gate potential of the current absorbing transistors of the succeeding stage can be used to provide the proper bias for the preceding stage. This avoids the use of the cascode stage for proper biasing except for the last stage.

Fig. 28 shows an embodiment of how folding cells containing the core of Fig. 19 can be cascaded to construct an analog-to-digital converter. Also here the comparators for determining which current path is taken by the input currents are omitted for simplicity. In the example, the reference currents needed at the input of each stage are provided using the cascodes which bias the previous stage by setting the Il and Ir in Fig. 24 equal to the reference required by the next stage. This way, the current folding cell of Fig.26 reduces to the circuit of Fig. 24 in this cascade.

The operation is analogous to the example with transistors only. The folded cascode stages allow to use the same reference for the inputs of all stages. One can also change the input current of the last stage with a δ to obtain a similar advantage as explained for the previous case. The output currents of the last stage are fed straight into the supplies, but could be fed into another type of current sink. Fig. 29 shows a block

diagram representation of the circuit of Fig. 28. Note that the magnitude of the reference currents belonging to a certain stage are annotated next to that stage, although the folded cascodes biasing the previous stage are providing this current. An asterisk on the last cell denotes that here the currents are fed straight into a current sink or power supply.

Fig. 30 shows a similar block diagram of a cascade, but where the bias currents are different. In addition, currents are added at the outputs of the last stage. The reason for this is explained below. Fig. 31 gives a block diagram representation of the circuit of Fig. 30. This block diagram is used to illustrate in Fig. 32 how an analog-to-digital converter can be constructed using several circuits shown in Fig. 30 in parallel. In the figure, the block diagram of Fig. 31 is used with omission of the arrows indicating the digital outputs in Fig. 30. Fig. 32 indicates that the input currents to the various cascades in parallel are offset with respect to each other. Fig. 33, 34, 35 and 36 show the magnitude of the currents at the outputs of the first, second, third and fourth stage in the cascades, respectively. The outputs of the last stage can be centred around zero by adding a current or they can also be offset slightly with respect to zero. The latter was done here by the current source added to the outputs of the fourth stage in the cascade of Fig. 30, while the former could have been done using $8*I_{lsb}$ instead of the $8.5*I_{lsb}$ and $7.5*I_{lsb}$ shown in Fig. 30. After this current addition, the resulting current outputs can be fed into another folding stage (with comparators) which injects its output currents into current sinks (i.e. as for instance in the example of Fig. 28 and 29). Alternatively, the outputs can be presented to current comparators.

In such configuration using a plurality of cascades as in Fig. 30, the least significant bits can be determined by establishing the cascade of which the output currents of the last stage were nearest to the zero crossing. The comparison signals of the last stage serve this purpose. The very significant advantage of this with respect to a configuration with only a single cascade, is that those output currents of the last stages only need to be accurate near the zero crossing, because that is what determines the least significant bits, and can be inaccurate further away from the zero

crossing of the last stage. One can therefore allow the current folding of the previous stages to be less accurate around their zero transition point. This means in practice that one can increase the zero-input current of those stages significantly, and therefore considerably increase the bandwidth of those stages. This will cause errors in the currents around the zero transitions of the previous stages because current is not conducted by one current path only. Only when one comes near to the zero transition of the outputs of the last stage of that cascade, do the currents need to be accurate. One has to therefore only guarantee that at that moment no significant current leaks away in the previous stages through current paths which are not supposed to conduct current at that moment. The concept that current folding cells are only accurate when needed and relatively inaccurate otherwise and that this may yield a speed advantage is novel and is therefore an object of the invention.

The more significant bits in such a configuration with a plurality of cascades of folding cells can be determined in several ways. One can select the most significant bits determined by the cascade of which the last stage is nearest to the zero crossing. The significant advantage here is that for those more significant bits it is known that one is far from the zero transition, and one can therefore afford the comparison signals from those previous stages to be less accurate around the zero transition point. They only need to be accurate when they are used to determine the bit code.

Another way to determine the most significant bits is by averaging the bit determining signals of the different cascades corresponding to those bits. This can easily be implemented by using a series of transconductors which each correspond to a certain bit or its complement of a certain folder. This is illustrated in Fig. 38. In the figure, the current folding cell corresponding to a particular bit in the first folder and last (n^{th}) folder are shown in more detail. The corresponding cells of the remaining folders and the connections of the transconductors they contain are identical. The currents of the transconductors all correspond to one particular bit or its complement. They can be summed to determine the value of that bit. This can be done as illustrated in the figure by connecting

their outputs together to obtain a positive and a negative output line. The current in these two lines has to be compared by means of an amplifier and a comparator or by some other way to determine the value of the bit. The use of these transconductors allows to implement some gain and some averaging to reduce the influence of offsets, while only having one comparator per bit.

One can also average in the digital domain, so one can decide to first carry out the comparison on the signals from the transconductors for instance, or compare directly the voltages at the inputs of the current folding cells. This would correspond to a majority voting scheme.

One can combine the averaging and the selecting technique, by selecting the average of the MSBs corresponding to a certain number of folders of which the current outputs of the last stage are nearer to the zero crossing than the others.

A further object of the invention is that, since the analog outputs of the current folding cell carry current, it is easy to combine those outputs. Usually this can be done by just connecting the wires together as illustrated in Fig. 39. One advantage for a configuration with several folders in parallel is that if current outputs are combined from cells in the different folders, the current presented to the next stage is larger and that hence the attainable speed for that next stage is increased.

A further advantage of the use of a plurality of folders is that the folder outputs can be combined and mutually compared. The result of the comparison can be fed back to the inputs of the folders to reduce or eliminate offset between folders. An example of how information can be obtained regarding offset between folders from the folder outputs is shown in Fig. 42, where a configuration with two folders in parallel is used. The folders are fed by two differential pairs which have the same input signal. This signal is related to the signal to be converted. The first output of the first differential pair is linked to the first input of the first folder, the second output of this first differential pair is linked to the second input of

the second folder. The first output of the second differential pair is presented to the first input of the second folder, and the second output of the second differential pair is presented to the second input of the first folder. In the example some offset was introduced for the first differential pair by means of a difference in the current sources A and B, A being linked to the first output of the first differential pair, B being linked to the second output of the first differential pair. A deliberate offset with the same magnitude but opposite sign was introduced in a similar way for the second differential pair, by means of a difference in the current sources C and D, C being linked to the first output of the second differential pair, and D being linked to the second output of the second differential pair. The thus introduced deliberate offset comes in addition to the random offset which might be different for the two differential pairs. Below it is explained how a difference in random offset can be derived from the folder outputs in Fig. 40.

In the example, the two folders each carry out five folding operations on the input signals. The output currents of the two folders after the fifth fold are plotted as a function of the input current delivered by one of the two differential pairs in Fig. 41 for the case where no random offset is present in the two differential pairs. The outputs of the two folders are mutually shifted due to the deliberately inserted offset, but have the same shape. Note that each of the two folders has an output where the output current has a positive sign, and one where the output current has a negative sign. In principle the sum of the two current outputs of each folder should be zero, so if one defines the signal "Corr" as the sum of the two output currents of the first folder minus the sum of the two output currents of the second folder, one would expect "Corr" to be equal to zero if no random offset is present. Fig. 41 also showing "Corr" confirms that it is equal to zero for the full current input range.

Fig. 42 plots the output currents of the two folders and the "Corr" signal for the case where the first differential pair has an offset equal to the offset of the second differential pair but opposite in sign. Now the output currents of the two folders are not only mutually shifted but

also have a different signal shape. The "Corr" signal is plotted as well and it can be observed to be different from zero now, but constant over the full current input range. In fact, the "Corr" signal is proportional to the difference in offset between the two differential pairs. Since it is constant over the full input range it can easily be used in a feedback loop to cancel this difference.

Fig. 43 shows an example of how to determine the "Corr" signal. The two output currents of each folder are injected into one branch of a differential circuit. The two currents are added in the branch, and the differential configuration of the two branches causes a voltage difference to be developed between the nodes "u" and "v" proportional to the "Corr" signal when "Corr" is not too large.

Fig. 44 illustrates how this potential difference between the nodes "u" and "v" can be used in a feedback loop to correct for the offset difference between the two differential pairs. A differential current proportional to the voltage difference between the nodes "u" and "v" (for a small difference) is added to the outputs of the first differential pair. A differential current equal in magnitude and opposite in sign is added to the outputs of the second differential pair. For a sufficiently large gain and a sufficient phase margin for the feedback loop, this circuit effectively eliminates the difference in offset between the differential pairs, and causes the circuit to behave as if the two differential pairs had an offset equal to the average of the real offset of the two differential pairs. So this circuit performs an averaging function. Note that the deliberate offset introduced between the two folders is not affected by the feedback circuit.

A further reduction of the offset – so also for the average offset of the two differential pairs – can be obtained by sampling the input current onto the same set of differential pairs. This is illustrated in Fig. 45. This approach guarantees that sum of the differential output currents of the two differential pairs is equal to the differential input current. This substantially cancels the average offset as the input voltages to the differential pair will adapt due to the sampling to absorb the full differential

input current. A difference in offset between the two differential pairs is not cancelled out by the sampling, however, but the feedback scheme described above can be used for this purpose. Since the combination of the sampling on the same differential pairs and the feedback circuit eliminate both the average and the difference in offset between the two differential pairs, the effect of this offset is fully eliminated by means of this circuit. The precision of this circuit is therefore limited by the precision of the folders and the current sources they contain themselves and not by the differential pairs. Note that a sufficiently large capacitance needs to be associated with the input nodes to reduce sampling noise. Fig. 45 illustrates how switches allow the input signal to be sampled on the input nodes, and after sampling to be applied to the two folders. When the sampled input is applied to the two folders, the time-varying input current is absorbed by a current sink.

In the previous example, the offset between different differential pairs was substantially eliminated by sampling the input signal onto the same set of different pairs. Another way to eliminate the effect of offset between different differential pairs is described by means of the example hereafter. The example is given for four differential pairs D1 to D4 and three folders FO1 to FO3 and is shown in Fig. 46. The circuit relies on the well-determined relationship between the two output currents of each folder, in particular that their sum is either substantially zero or a constant in case some deliberate offset is introduced. This can be used advantageously in the following way. The input current to be converted is applied with one sign to a first differential pair D1, of which the transistor receiving the current on its drain and gate is diode-connected. The input current is also applied with the opposite sign to a second differential pair D2, also with the transistor receiving the signal being diode-connected, i.e. with its gate connected to its drain. Note that in practice some buffering can be applied in between the drain and the gate of the input current absorbing transistor to minimize the capacitive load seen by the input signal. The gate of the other transistors in the two differential pairs D1 to D2 is connected to a reference. The input current (or the positive and the negative component of the differential input signal) will cause a voltage to

develop on the gate and drain of the receiving transistors dependent on the input signal. This voltage can also be applied to other differential pairs; in the example with four differential pairs, the third differential pair D3 receives the same voltages on the gates of its two transistors as the first differential pair D1, and the fourth differential pair D4 the same voltages on the gates of its two transistors as the second differential pair D2. Three folders are linked to the outputs of these four differential pairs in the following way: Folder FO1 receives as input currents the available output current of the first differential pair D1 (corresponding to the transistor which is not diode-connected) and the first output of the third differential pair D3. This first output of the third differential pair D3 is the one which is supposed to carry a current equal in magnitude but opposite in sign to the one carried by the available output of the first differential pair. In the same way, the second folder FO2 receives as input currents the available output of the second differential pair D2 and the output of the fourth differential pair D4 whose current has the opposite polarity to the one of the available output of the second differential pair D2. The third folder FO3 receives as input currents the second output current of the third and fourth differential pair D3 and D4.

If the currents supplied by the current sources to the differential pairs are sufficiently well controlled, the current applied to the first input of the first folder is substantially equal to the input current applied to the diode-connected transistor of the first differential pair, or to this current plus a well-defined deliberately introduced constant offset, determined by the current source linked to the available output of the first differential pair. Since the sum of the input currents – and hence the sum of the output currents – of the first folder has to equal a predetermined value – either zero or a constant – this condition can be imposed using a feedback loop acting on the current sources linked to the outputs of the third differential pair D3. In the figure, this feedback is schematically indicated by the ellipse around the two outputs of folder FO1 and the arrow pointing to the current sources feeding the differential pair D3. If the sum of the current outputs of the first folder FO1 is different from the predetermined value, a corrective signal is applied to the current sources of the third differential

pair D3, until the sum substantially equals the required value. This substantially eliminates the offset between the first and the third differential pair D1 and D3. Similarly, a feedback loop can be used to eliminate the offset between the second and the fourth differential pair D2 and D4. This feedback loop is schematically indicated in Fig. 46 in a similar way as the first feedback loop.

The sum of the input currents – and hence the output currents – of the third folder should also equal a certain predetermined value. Also here this can be used for a feedback loop, in particular to provide a common mode cancellation signal for the two current inputs. The sum of the output currents of the third folder will act as a corrective signal for the current sources applied to the diode-connected transistors in the first and second differential pairs D1 and D2. This corrective signal will make the sum of the output currents of the third folder constant and this will effectively cancel the common mode between the two input currents to the full system should the match between the input currents I_{in} and $-I_{in}$ not be exact. This feedback is schematically indicated in the figure in a similar way as the previous two feedback loops. Please note that the feedback in this case is in common for the two current branches to which it is applied. The first two feedback loops applied a differential feedback between two branches.

Fig. 47 gives an example of how the three feedback loops schematically shown in Fig. 46 can be implemented in practice. The sum of the output current of each folder is formed using a cascode circuit. If the sum of f1 and f1- is different from zero, the node p will be charged or discharged, and since this node p controls the output of the PMOS differential pair adjusting the offset of the differential pair D3, the offset will be corrected. $V_{ref}2$ controlling the other input terminal of this PMOS differential pair is a fixed reference in this example. The node q is charged or discharged in a similar way if the sum of f2 and f2- is different from zero, and this will correct for random offset in the differential pair D4. Finally, if the sum of f3 and f3- is different from zero, the node r will be charged or discharged. This will cause a corrective signal to be applied to

the two current inputs of the circuit to eliminate common mode between the two current inputs I_{in} and $-I_{in}$, should they not have been substantially equal and opposite in sign.

In conclusion, the fact that the sum of the input currents and hence the sum of the output currents of one folder is equal to a predetermined constant value in this example, allows to apply feedback to effectively eliminate the offset between differential pairs and the common mode in the input signal. Since therefore the size of the transistors in the differential pairs can be reduced to a minimum (their offset will be cancelled anyway), the parasitic capacitance associated with these transistors can be severely reduced resulting in a substantial speed advantage. Note that standard methods known to people skilled in the field have to be applied to guarantee stability for this feedback configuration.

These were examples with a small number of parallel folders and differential pairs. This principle of reducing or eliminating random offset based on the relation between the outputs of the folders can be more generally applied for the configuration with a larger number of parallel folders, and can also be used to reduce offset between folders generated by circuits other than differential pairs, for example current mirrors. This principle can also be applied in a cascade configuration. For instance, in the example of Fig. 46, differential pairs could be added with their inputs connected to the inputs of the last stage of the folders, so they would sense the input voltage to the last stage of the folders. Several differential pairs could be added per folder, and one could present their outputs to current folders again, and then correct their offset based on the fact that they received the same input and on the relation between folder outputs.

This principle of reducing or eliminating random offset is based on the relation between the multiple outputs of one or more folders. It offers the possibility of eliminating offset at the folder inputs using a simple feedback scheme. Prior art techniques either only offered an offset reduction due to averaging for instance, or introduced considerable circuit complexity using for instance chopper amplifiers and digital filtering.

Therefore this technique to reduce or eliminate random offset constitutes an improvement over the prior art and is therefore an object of the invention.

In some applications, several signals which have some well-defined relationships have to be converted at the same time. In that case, feedback loops which act on several converters at the same time can be envisaged to correct or reduce deviations from this well-defined relationship. These feedback loops would detect deviations in folder outputs or combinations of folder outputs from the expected value and apply a corrective signal to the converter inputs.

A further object of the invention is that a track-and-hold or a sample-and-hold circuit can be inserted in-between stages in the cascade of folding cells to construct a pipelined analog-to-digital converter. This would allow the conversion speed to be increased, as the current needs to traverse a smaller number of stages during each clock cycle. In fact, the folders constructed from the new current folding cell described here automatically generate a residue between the value represented by the bits determined in the folder and the input value. Therefore these folders are particularly suited for switched current applications also when the input signal is oversampled.

Also a gain stage can be inserted in between some of the stages in the cascade of current folding cells to increase the conversion speed. This is illustrated in Fig. 48 where a current mirror is used to amplify the current. The advantage of such schemes is that the currents in the stages subsequent to the gain stage are increased yielding a higher bandwidth for those stages. The disadvantage – as is the case for the current mirrors – is that mismatch in the gain stage is introduced. This mismatch has to be sufficiently small to match the resolution specification of the converter, and this might lead to the requirement for large devices, which would slow down the gain stage. An alternative solution is to use the corrective scheme above to either cancel or reduce the introduced mismatch.

A further object of the invention is that the current outputs of the current folding cell can be used to directly determine the value of bits less significant than the one determined in the current folding cell itself. This is illustrated by an example in Fig. 48. In the example, the output current of the folding cell (which can be the last folding cell in a cascade of folding cells) is presented to a resistor. The voltage developed across this resistor is compared to several reference voltages by means of comparators. The generation of the reference voltages used for this purpose is illustrated by way of example in the figure. A reference current I_{ref} is injected into a series string of four resistors. The voltages developed at the terminals of the resistors are the reference voltages for the voltage comparators. If the value of the resistors in the series string and that to which the output current of the folding cell is presented are chosen to be the same, the comparators will detect whether the output current of the folding cell is smaller or larger than I_{ref}, $2*I_{ref}$, $3*I_{ref}$ and $4*I_{ref}$, respectively.

So far, current folding cells and their use for analog-to-digital converters have been discussed. However, these current folding cells can also be advantageously used for mixers. An example of this is shown in Fig. 50, where in addition to a signal current I_{signal} at the first input and a signal current $-I_{signal}$ at the second input a current I_{mix} is applied which alternates between the two inputs. If I_{mix} is larger than twice the range of the signal current, it will determine which of the two input signal current is transferred to the first and the second output of the folding cell. The advantage of this cell is that there only is a transfer of the signal current from one of the two outputs to the other and back as the clock alternates. There is no signal transformation as for instance a current-to-voltage conversion and back, which would be dependent on component non-idealities and mismatch. In addition, it could be linked directly to an analog-to-digital converter as previously described so that the full chain could fully operate on current minimizing the signal distortion.

The novel current folding cell introduced here allows the implementation of an analog-to-digital converter with a very limited number of components. This allows the introduction of some additional circuit to

compensate for or severely reduce the influence of parasitic capacitances in the current path of the time-varying signals. Fig. 51 shows a prior art circuit to reduce the influence of a parasitic capacitance linked to the node X1. The output of the buffer in the circuit, which is connected to the other electrode of the parasitic capacitance C_{par}, ideally follows the potential of the node X1, effectively reducing the capacitive current through C_{par} to zero. In practice, the buffer is not infinitely fast, nor does it have an infinitely high loop gain, both resulting in its output only approximately following the input. This will result in a beneficial reduction of the capacitive current in C_{par}, but not in a full cancellation.

Fig. 52 shows an alternate circuit which has the same purpose. Here the capacitive current is lead back to the node X1 by means of a cascode transistor. The source of the cascode transistor is linked to the other electrode of the parasitic capacitance C_{par}, and the drain of the transistor is linked to the node X1 of which one would like to reduce or eliminate the influence of the parasitic capacitance C_{par}. The cascode transistor will try to maintain a constant voltage on its source, and will therefore try to transfer any current it receives on its source to its drain. Note that here the capacitive current through C_{par} is not reduced. It is only directly fed back to the node X1, which therefore will see a reduction of its capacitive lead due to the cancellation of the capacitive current through C_{par} by the drain current of the cascode transistor. Also here there are practical limitations, which will result in only a beneficial reduction and not a full cancellation of the capacitive load on X1 represented by the parasitic capacitance C_{par}.

Another way of reducing the influence of the parasitic capacitance is shown in Fig. 53. Here the buffer re-injects the capacitive current through a capacitor C_{par}' ideally equal to C_{par} back into the node X1, but with the opposite sign, effectively cancelling the capacitive current through C_{par}. In practice, the capacitive current is not perfectly cancelled due to the non-idealities in the buffer and in the matching off between C_{par} and C_{par}'. The advantage of this circuit is that it can be used even if the potential of the other electrode of C_{par} has to be kept at a fixed potential.

The circuits previously shown cancelled the capacitive current of a node X1 at the node itself. In a current processing circuit this is not always necessary nor convenient. It can be sufficient to re-inject the capacitive current into a node further along the same current path. Fig. 54 shows an example of this. In the figure, there is some current conducting element in the current path between the node X1 and the node X2. The capacitive current through a parasitic capacitance C_{par} on node X1 is re-injected into X2 through the cascode transistor. The circuit of Fig. 54 can be used if the potential of the other electrode of C_{par} is allowed to move. Fig. 55 illustrates a circuit using a buffer, allowing the circuit to be used even if the potential of the other electrode of C_{par} has to be kept at a fixed potential. Note that the unity gain buffer can be replaced by a non-inverting amplifier with a gain different from 1 if then the value of C_{par}' is adjusted to match the cancelling current to the original capacitive current. The capacitive current can also be measured by a charge amplifier and re-injected with the opposite sign into X1 or X2, provided the other electrode of C_{par} is allowed to move.

Another example of a case where the capacitive current is re-injected into a different node along the current path is when a parasitic capacitance is present between two different nodes along the current path.

Claims

1. Current folding cell comprising:
a plurality of current inputs,
a plurality of current outputs,
a plurality of current paths between said current inputs and said current outputs, each path comprising at least one non-linear element,
wherein the current path taken by each input current depends on the sign and/or on the magnitude of said input current,
characterized in that said non-linear elements are biased such that at least one of said input currents is different from zero when it changes from one current path to another.

2. Current folding cell according to claim 1, further comprising comparison means yielding at least one digital output representative of the sign and/or magnitude of said input current.

3. Current folding cell according to one of the claims 1 or 2, comprising a first current input and a second current input,
a first circuit (C1) providing two alternate current paths for the first input current (I1),
a second circuit (C1) providing two alternate current paths for the second input current (I2),
each of said current paths comprising at least one of said non-linear elements,
a first current summing circuit for adding the current from one of the current paths of said first circuit with the current from one of the current paths of said second circuit and for providing the result of the addition to said first current output,
a second current summing circuit for adding the current from the other current path of said first circuit with the current from the other current path of said second circuit, the output of said second current summing circuit being connected to said second current output and for providing the result of the addition to said second current output.

4. Current folding cell according to claim 3, wherein the input current (I_{in}) in said first circuit is equal in magnitude and opposite in sign to the input current ($-I_{in}$) in said second circuit.

5. Current folding cell according to one of the claims 3 or 4, further comprising at least one current summing circuit where more than one current arrives, the output of said current summing circuit being connected to one of said current inputs.

6. Current folding cell according to one of the claims 3 to 5, further comprising a first comparison means yielding one digital output indicating the path taken by said current in said first circuit, and second comparison means yielding a second digital output indicating the path taken by said current in said second circuit.

7. Current folding cell according to claim 6, wherein said comparison means comprise a multi-level comparator yielding a plurality of bits representative of the sign and/or amplitude of at least one of said input currents.

8. Current folding cell according to claim 4, wherein the output of one of said comparison means is only used for testing said cell.

9. Current folding cell according to one of the preceding claims wherein at least one of said non-linear elements is constituted by a transistor.

10. Current folding cell according to one of the preceding claims, further comprising a biasing circuit (B1) for biasing said non-linear elements in each path with a bias current (IDC) sufficiently high compared to the input currents to have two elements conduct when a small non-zero input current is presented to the input.

11. Current folding cell according to one of the claims 3 to 10, wherein different biases (u1, u2; d1, d2) are applied to said non-linear elements in the two circuits (C1) in the cell.

12. Current folding cell according to one of the preceding claims wherein at least one of said non-linear elements is constituted by a diode or by a diode-connected transistor.

13. Circuit comprising a plurality of current folding cells according to one of the preceding claims, said current folding cells being connected in cascade.

14. Circuit according to claim 13, further comprising at least one amplification stage between two cascaded folding cells.

15. Circuit according to claim 14, wherein said amplification stage includes a current mirror to amplify the current flowing from one stage to the next one.

16. Circuit according to one of the claims 13 to 15, wherein the bias current applied to the most significant cells in the cascade is such that the DC-current in the non-linear elements in each path is higher than what would be needed to reach the precision of current detection of the least significant stage or stages.

17. Circuit comprising a plurality of current folding cells according to one of the claims 1 to 11, wherein said current folding cells operates in parallel on signal of same significance.

18. Circuit comprising a plurality of current folding cells operating in parallel on signal of same significance

19. Circuit comprising a plurality of cascades of current folding cells operating in parallel on signal of same significance

20. Current processing circuit comprising at least one re-injection circuit for reducing the influence of a parasitic capacitance linked to a node by re-injecting in a node a current equal to the capacitive current, but with an opposite sign.

21. Circuit according to claim 20, wherein said re-injection circuit re-injects said current into a different node along the current path.

22. Circuit with a plurality of outputs whose levels are supposed to have a well defined relationship, comprising:
level detection means for detecting the level of each of said output,
verification means for verifying this relationship,
feed-back means for correcting this relationship by acting on said circuit and/or on the input signal of said circuit.

23. Circuit according to claim 22, wherein said outputs are current outputs.

24. Circuit according to claim 23, wherein said level detection means comprise:
a load after said output,
and comparing means for comparing the voltage loss over said load to a reference.

25. Circuit according to claim 23, wherein said level detection means comprise a load after said output, wherein said verification and feed-back means make use of the current after said load which is fed back into said circuit in order to adjust said relationship.

26. Analog-to-digital converter comprising a circuit according to one of the claims 13 to 25.

27. Analog-to-digital converter comprising a plurality of cascades of current folding cells according to one of the claims 1 to 12, wherein at least one bit of the digital output of the converter is derived from a plurality of

outputs provided by folding cells of the same order or significance in different cascades.

28. Analog-to-digital converter according to claim 27, wherein said outputs are outputs currents.

29. Analog-to-digital converter according to claim 28, wherein said output currents provided by folding cells of the same order in different cascades are summed, the result of said sum being used for determining said one bit.

30. Analog-to-digital converter according to claim 29, wherein a majority voting scheme is used for deriving said one bit from a plurality of output currents provided by folding cells of the same order in different cascades.

31. Analog-to-digital converter according to claim 30, wherein said at least one bit is derived from a plurality of output currents provided by one or several selected folding cells of the same order in different cascades, wherein only the folding cells corresponding to the cascade or cascades of which the current outputs are nearer to the zero crossing are selected.

32. Analog-to-digital converter according to one of the claims 26 to 31, further comprising mismatch compensating means for reducing the undesired mismatch between folding cells in different cascades or between the input signals of said cascades.

33. Analog-to-digital converter according to claim 32, wherein said mismatch compensating means comprise means for comparing the output currents of each of said cascades and feed-back means for adjusting the mismatch in said cascades depending on the result of the comparison.

34. Analog-to-digital converter according to claim 32, wherein said mismatch compensating means comprise a load after a stage in said cascade, said comparison means comparing the voltage loss over said load

with a reference, the current after said load being fed back in order to adjust said mismatch.

35. Analog-to-digital converter according to one of the claims 26 to 34, further comprising a track and hold circuit between at least some stages in the cascade of folding cells to construct a pipelined analog-to-digital converter.

36. Analog-to-digital converter according to one of the claims 26 to 35, further comprising means for measuring the output current of the last folding cell in said folding cell.

37. Mixer comprising a plurality of current folding cells according to one of the claims 1 to 12, said current folding cells being connected in cascade.

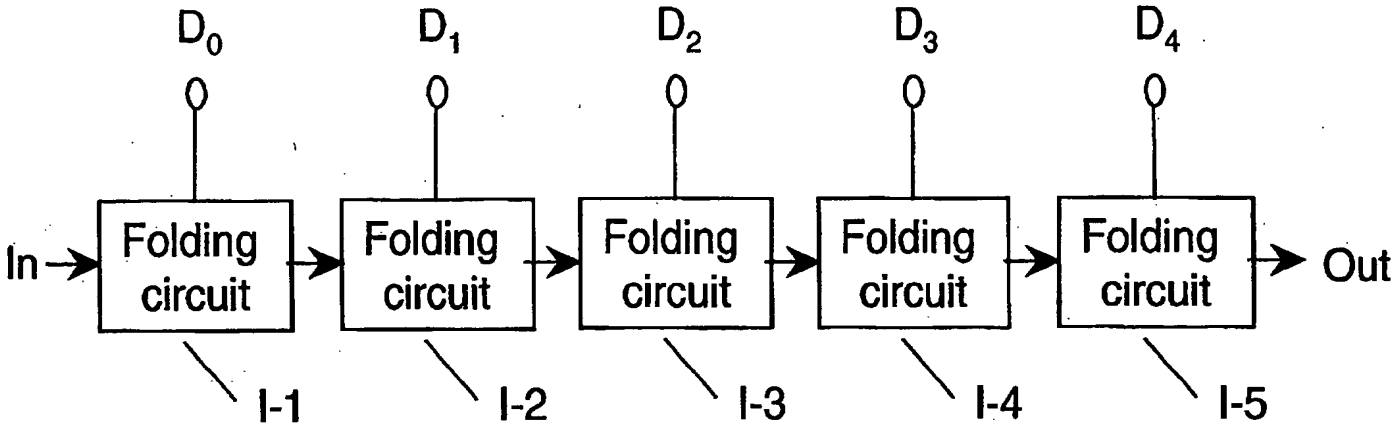


Fig. 1

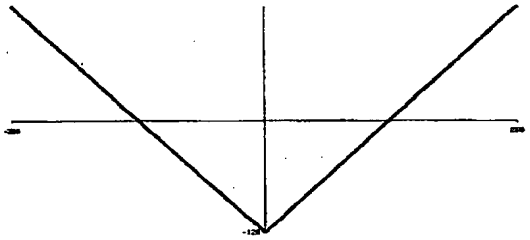


Fig. 2a

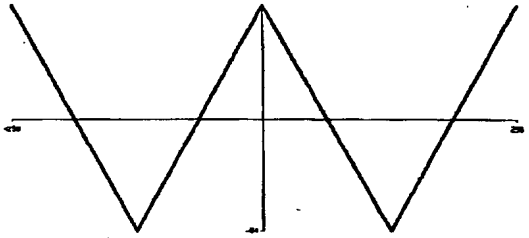


Fig. 2b

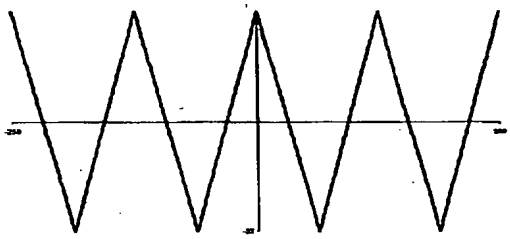


Fig. 2c

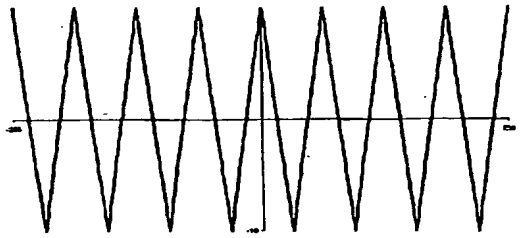


Fig. 2d

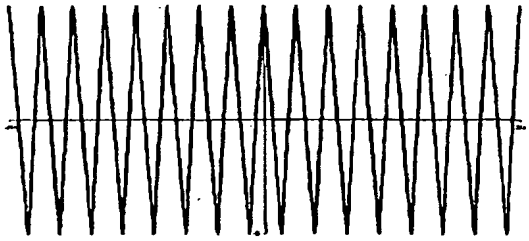


Fig. 2e

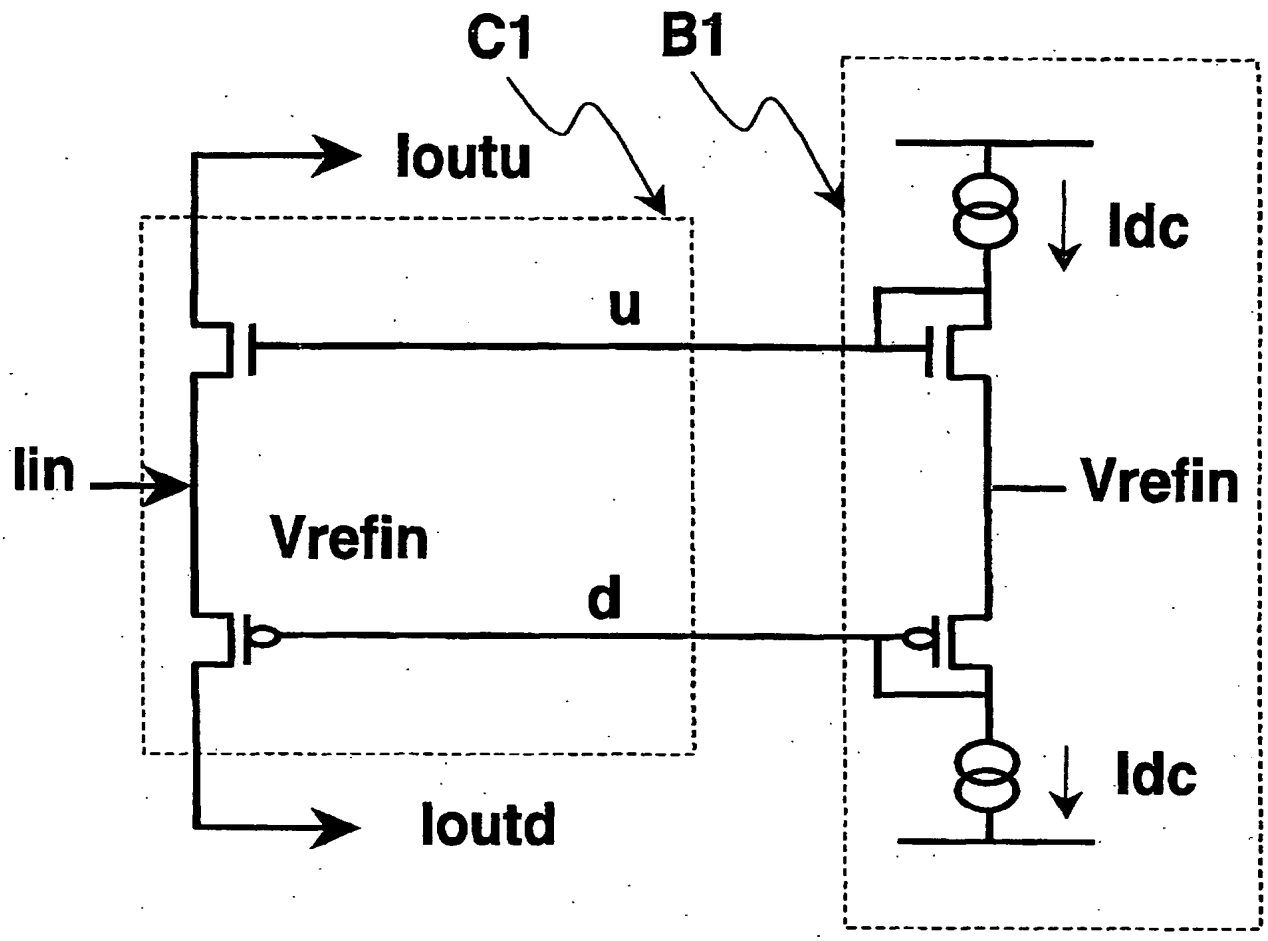
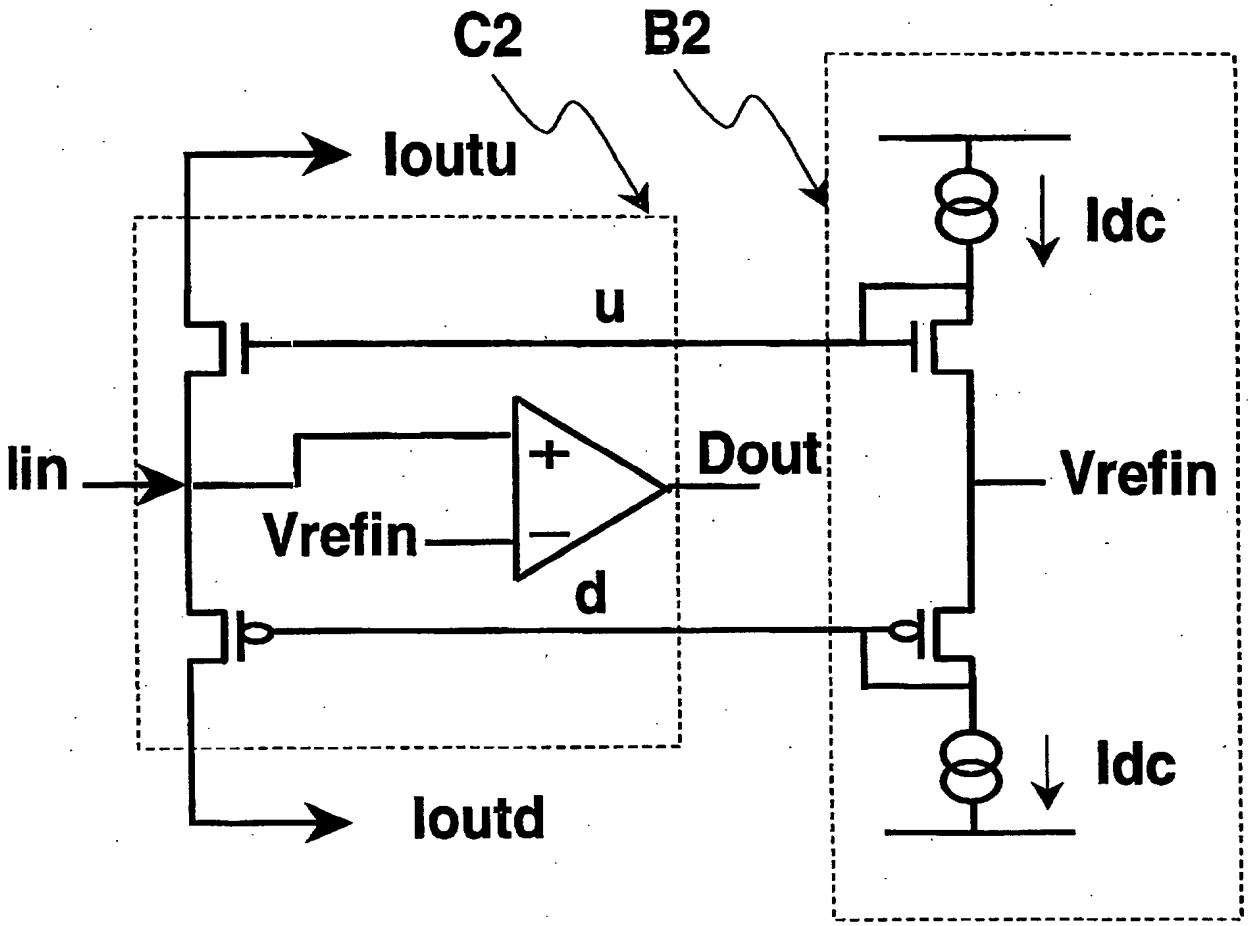


Fig. 3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B2
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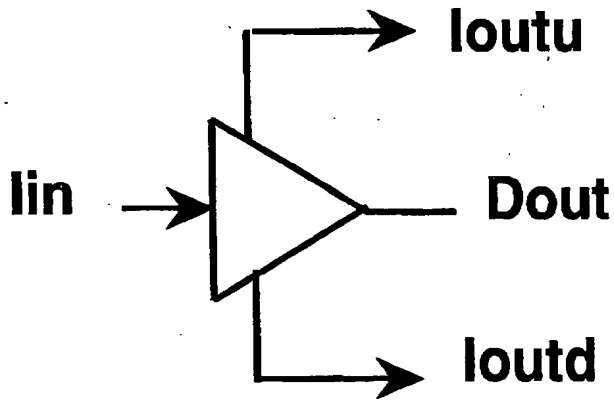
Idc
u
lin
Dout
Vrefin
Vrefin
d
Idc
Ioutd

Fig. 4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Dout
Ioutd

Fig. 5

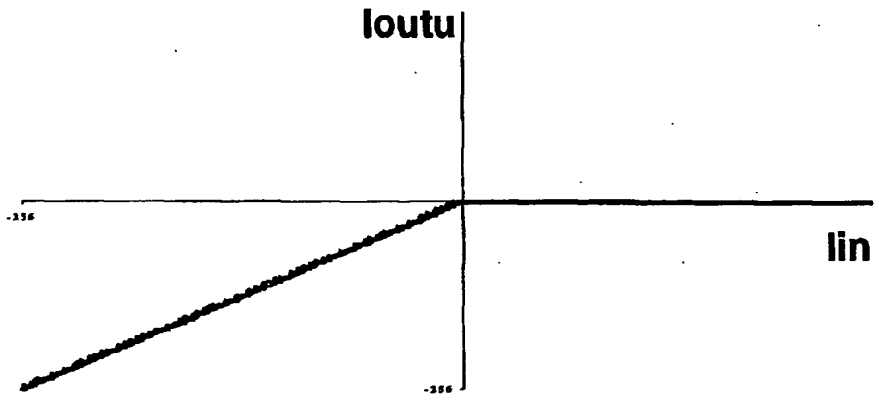


Fig. 6a

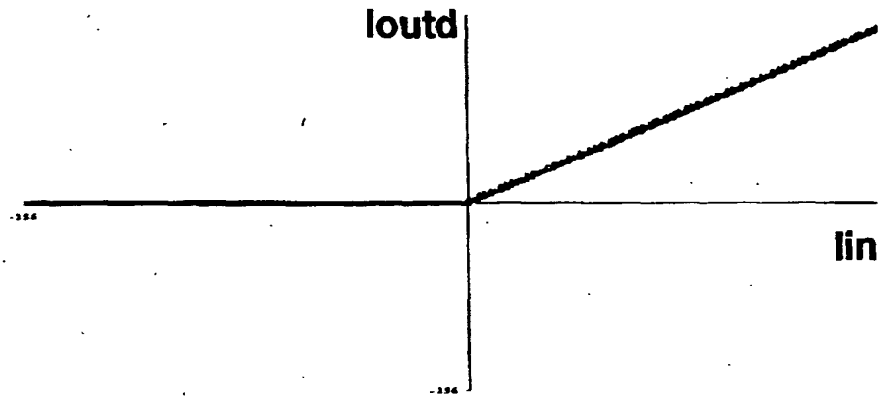


Fig. 6b

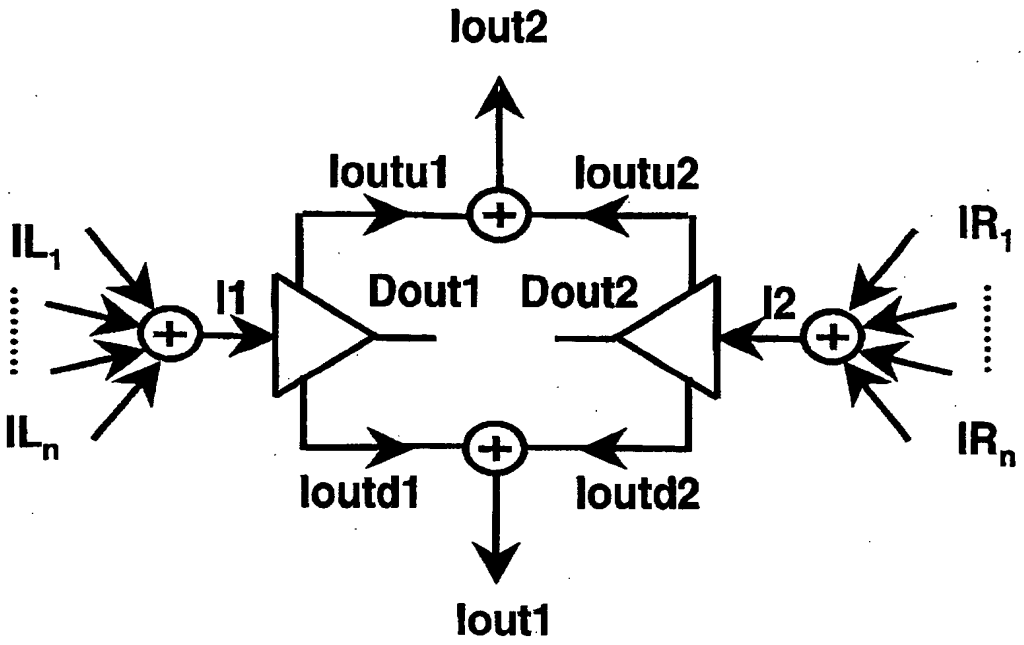
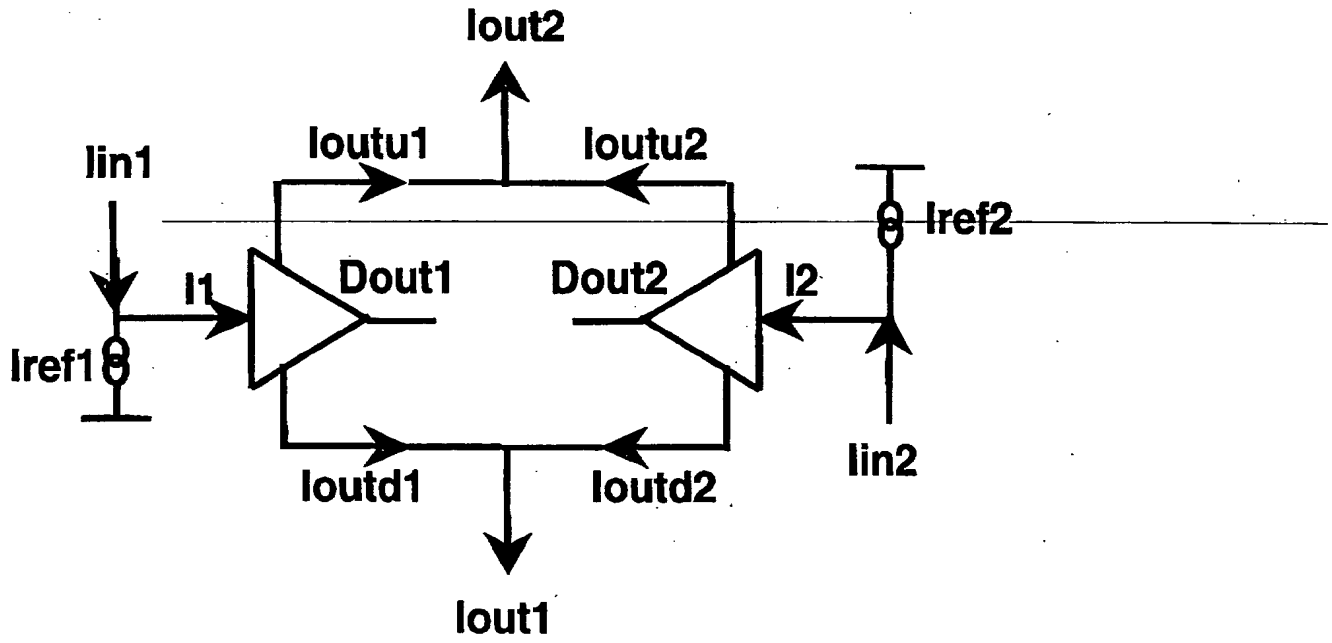

Iout2
Ioutu1
Ioutu2
IL1
ILn
I1
Dout1
Dout2
I2
IR1
IRn
Ioutd1
Ioutd2
Iout1

Fig. 7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Ioutu2
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Iref2
I1
Dout1
Dout2
I2
Iref1
Iin2
Ioutd1
Ioutd2
Iout1

Fig. 8

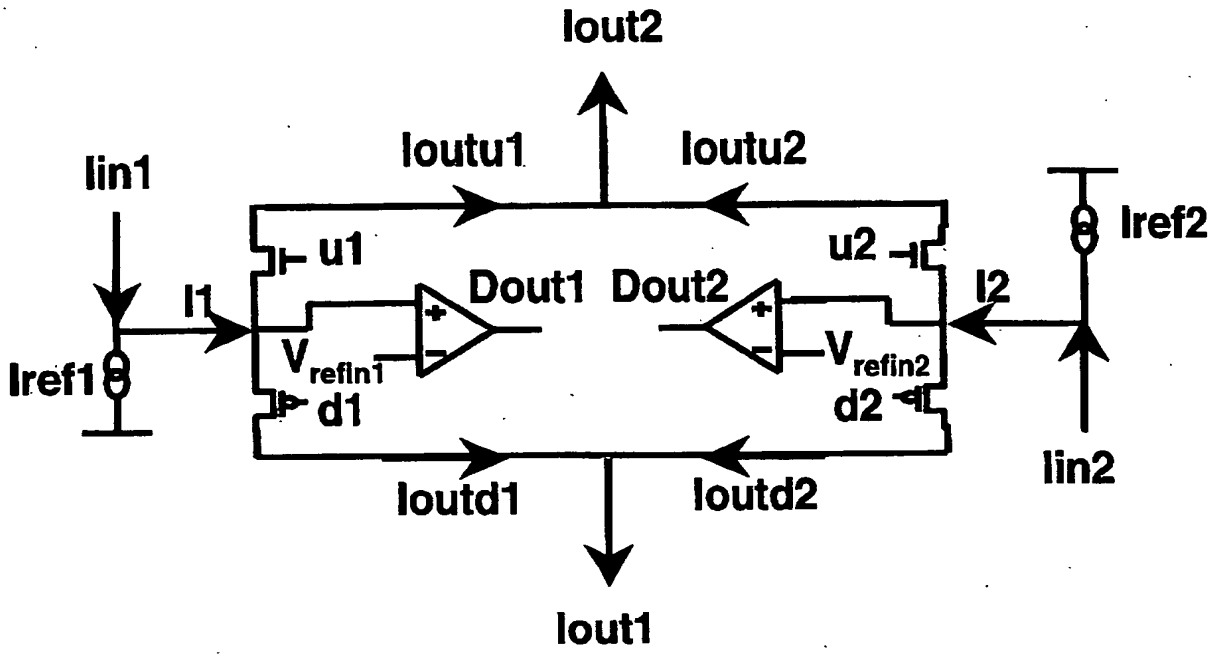

Iout2
Ioutu1
Ioutu2
Iin1
u1
u2
Iref2
I1
Dout1
Dout2
I2
Iref1
Vrefin1
Vrefin2
d1
d2
Iin2
Ioutd1
Ioutd2
Iout1

Fig. 9

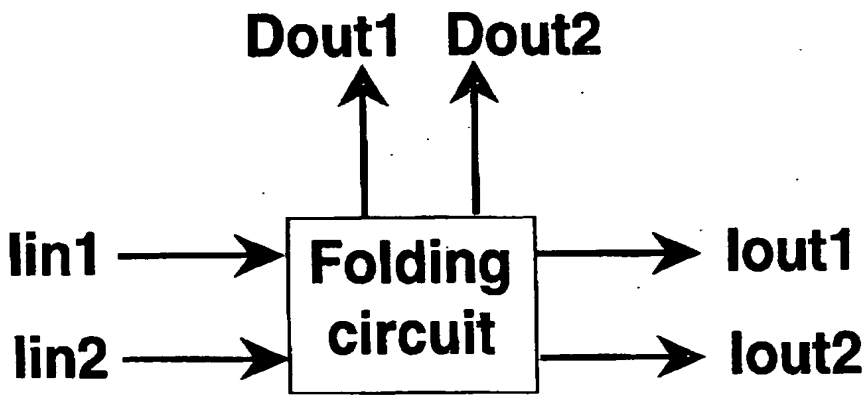

Dout1
Dout2
Iin1
Folding circuit
Iout1
Iin2
Iout2

Fig. 10

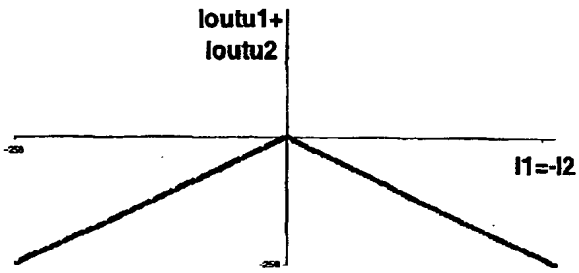


Fig. 11

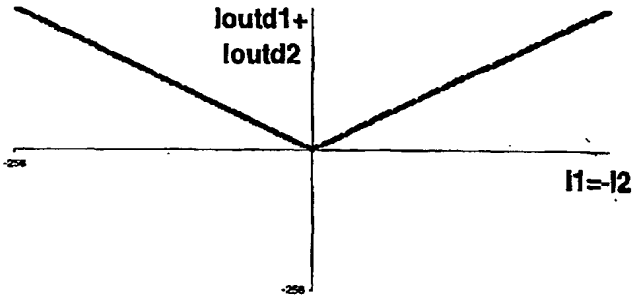


Fig. 12

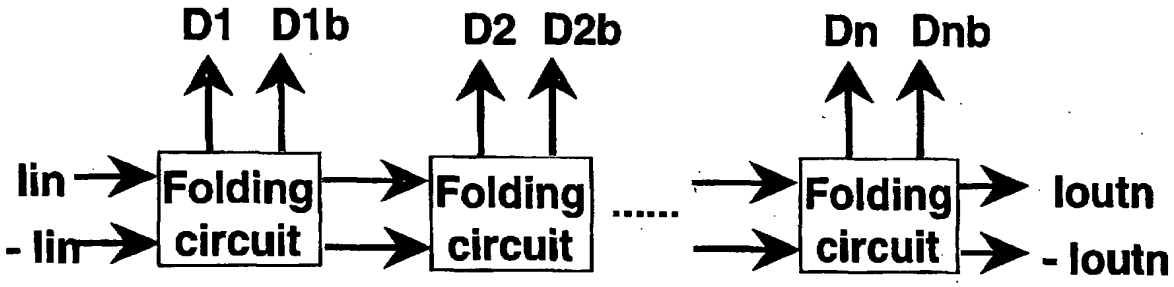


Fig. 13

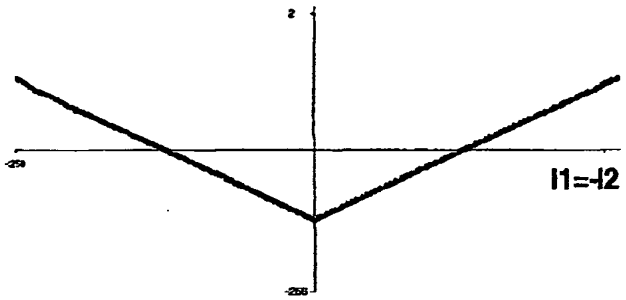


Fig. 14

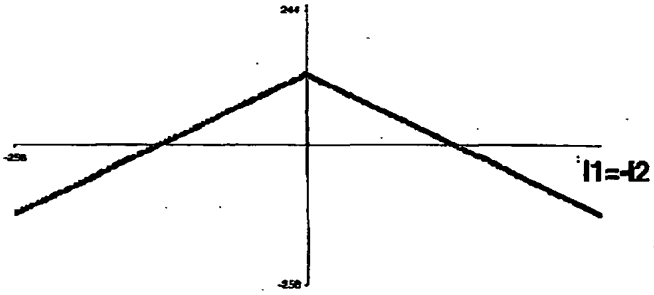


Fig. 15

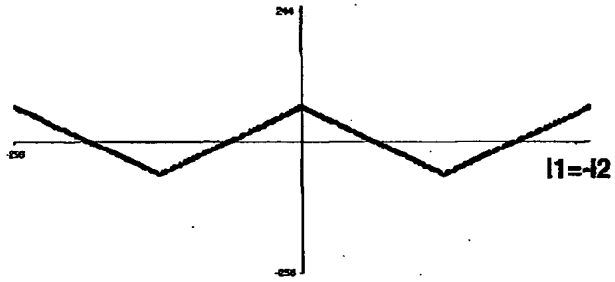


Fig. 16

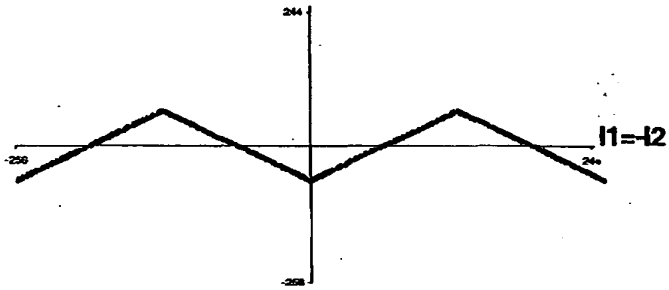


Fig. 17

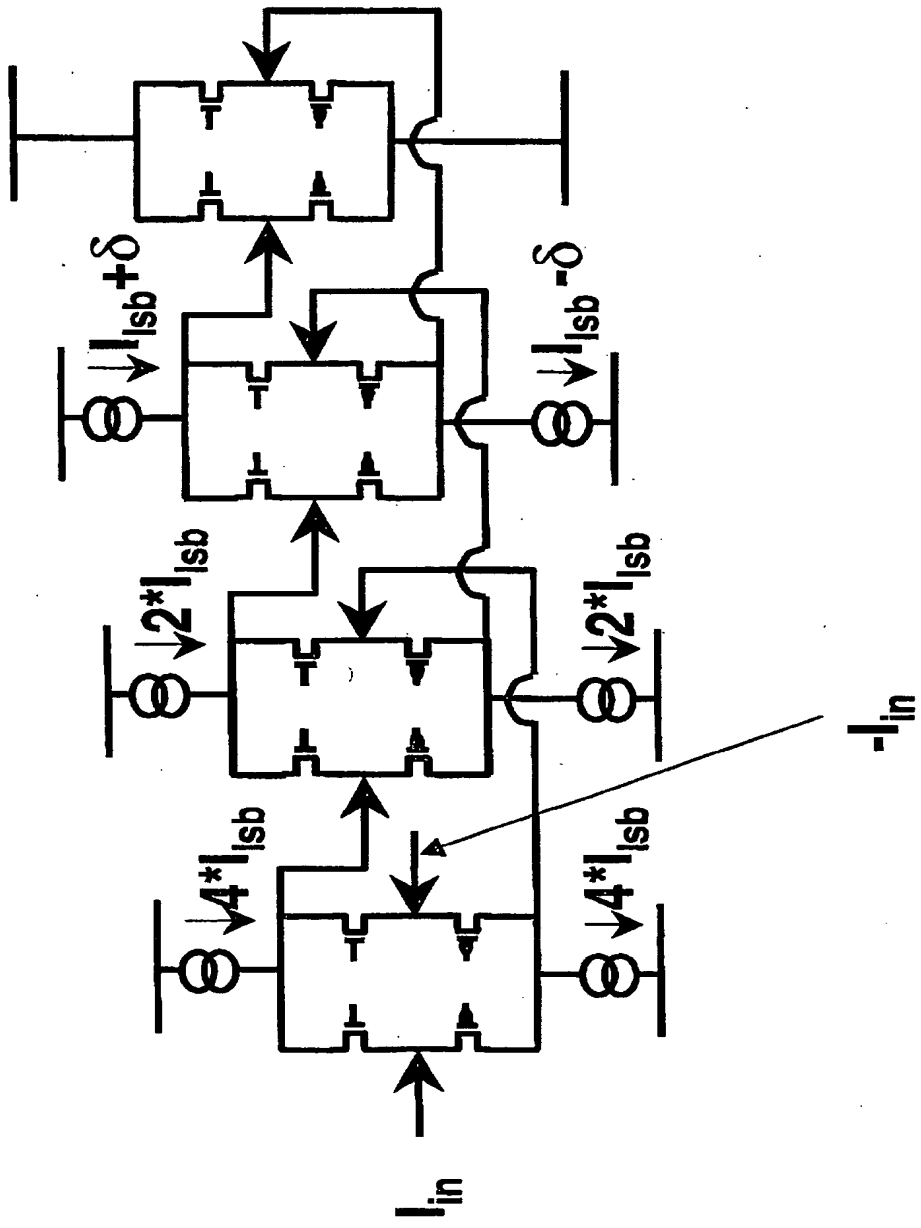


Fig. 18

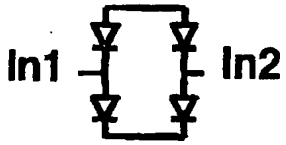


Fig. 19

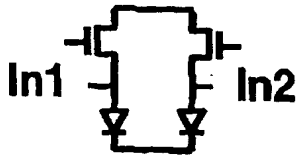


Fig. 20

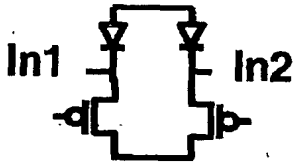


Fig. 21

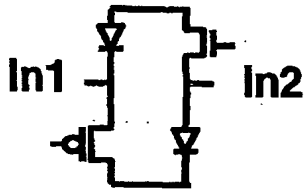


Fig. 22

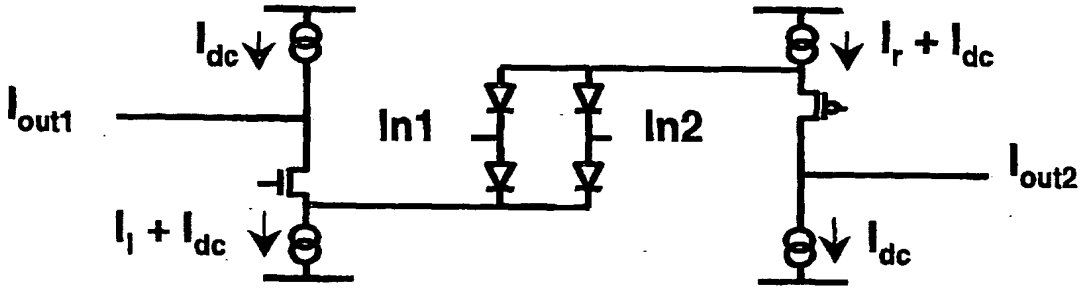


Fig. 23

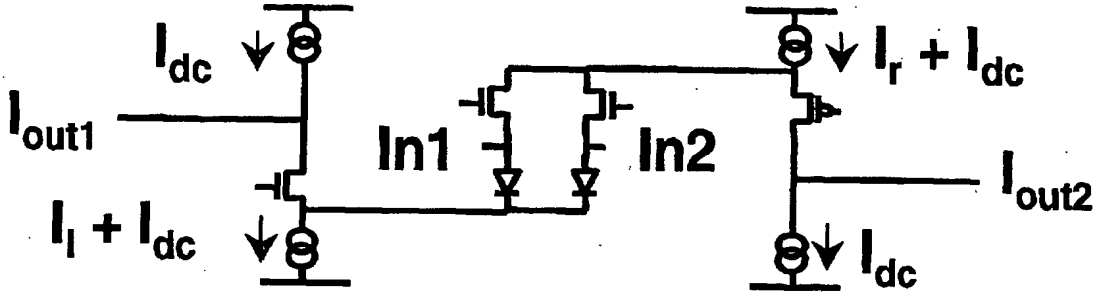


Fig. 24

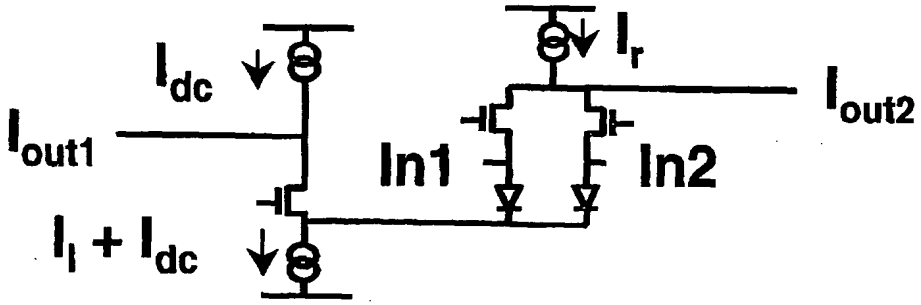


Fig. 25

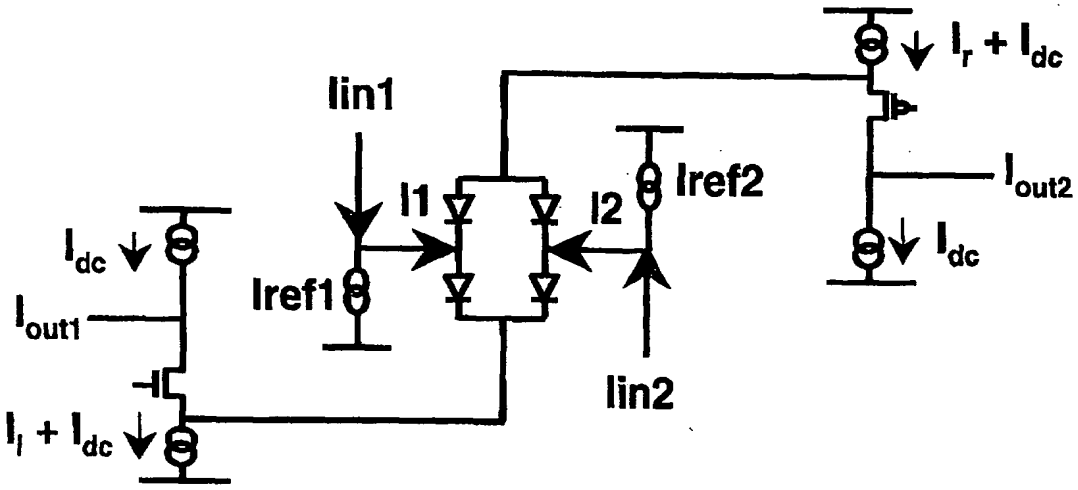


Fig. 26

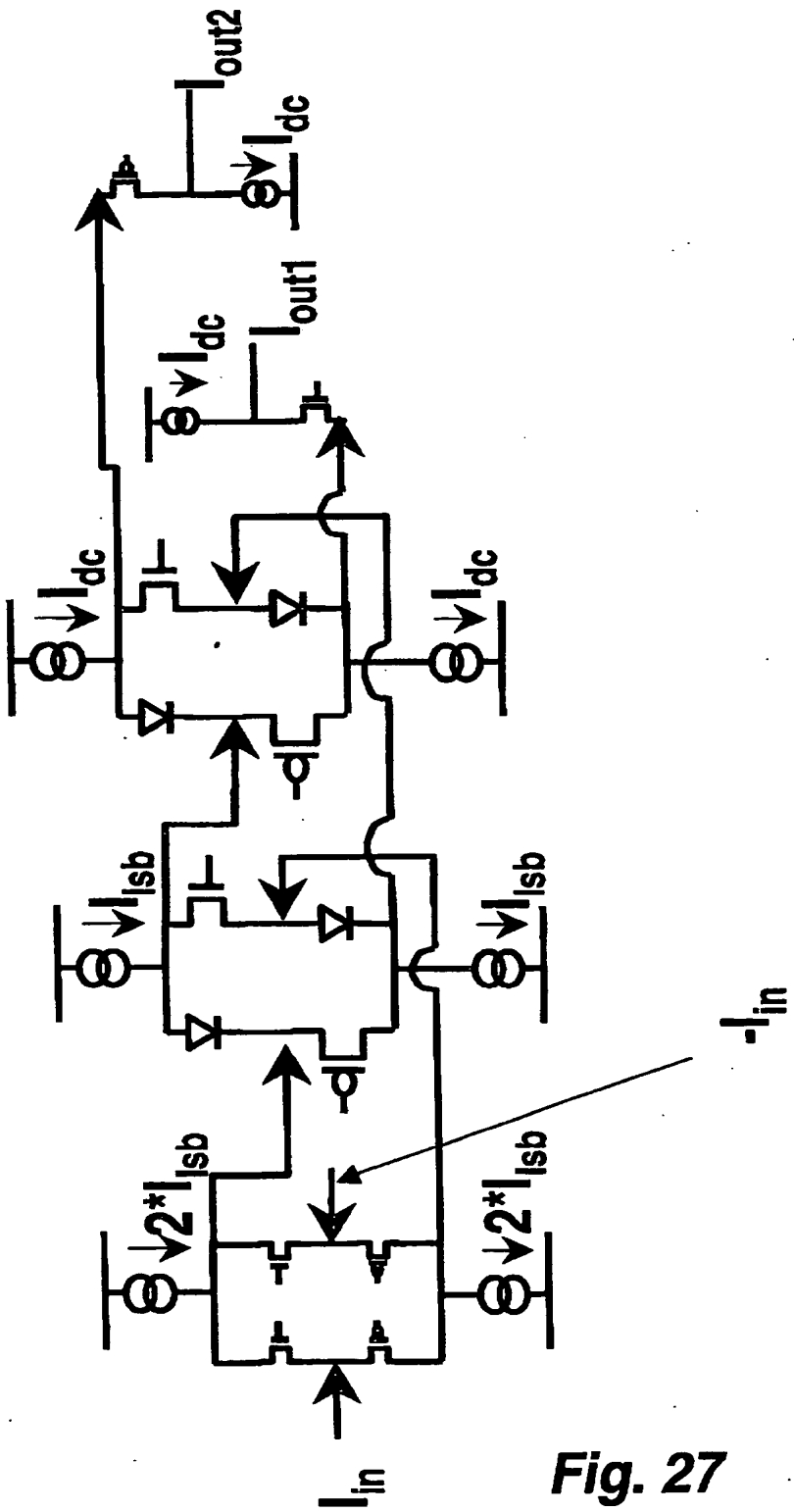
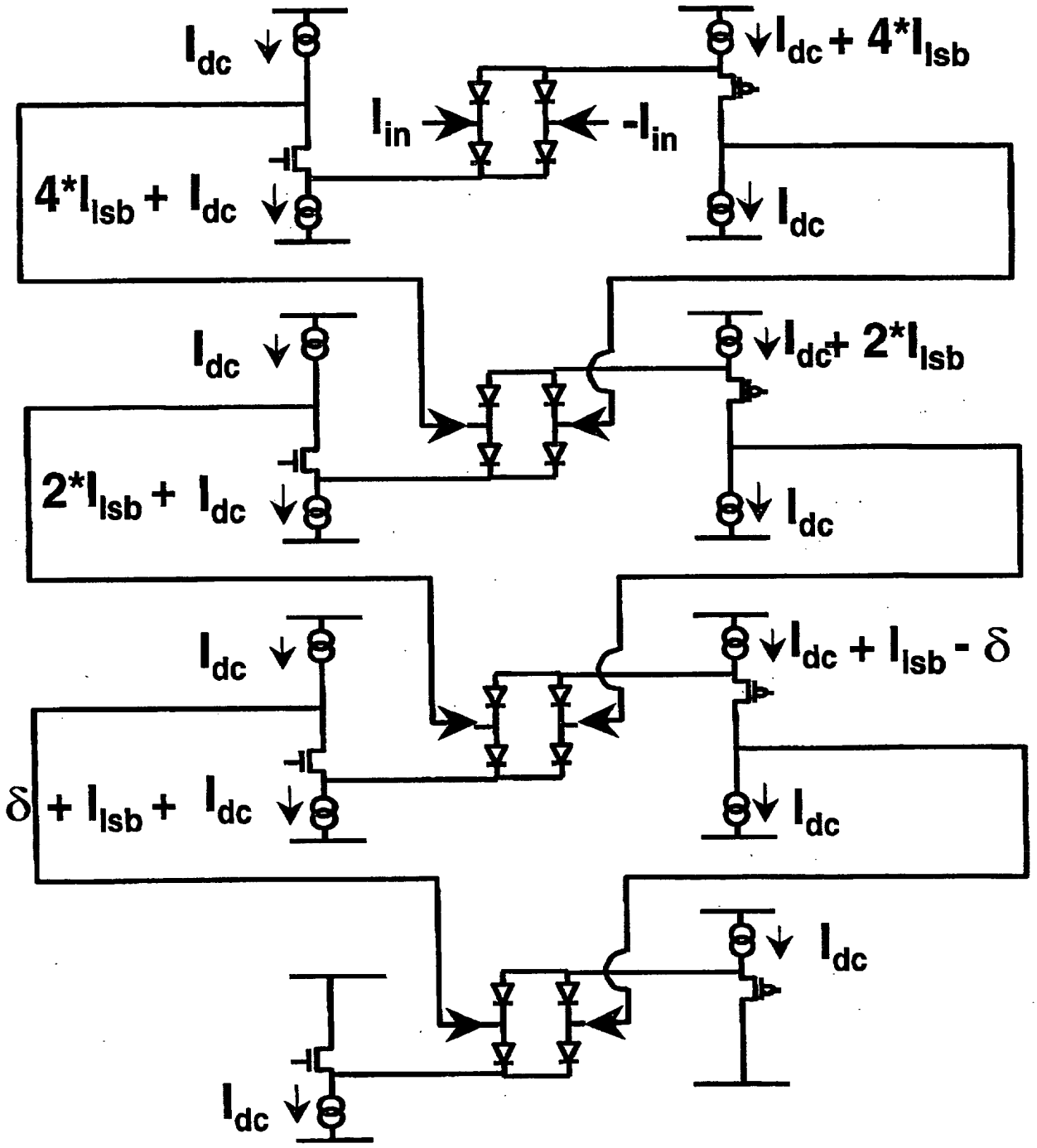


Fig. 27


I_{dc}
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I_{in}
$-I_{in}$
$4*I_{lsb} + I_{dc}$
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I_{dc}
$I_{dc} + 2*I_{lsb}$
$2*I_{lsb} + I_{dc}$
I_{dc}
I_{dc}
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$\delta + I_{lsb} + I_{dc}$
I_{dc}
I_{dc}
I_{dc}

Fig. 28

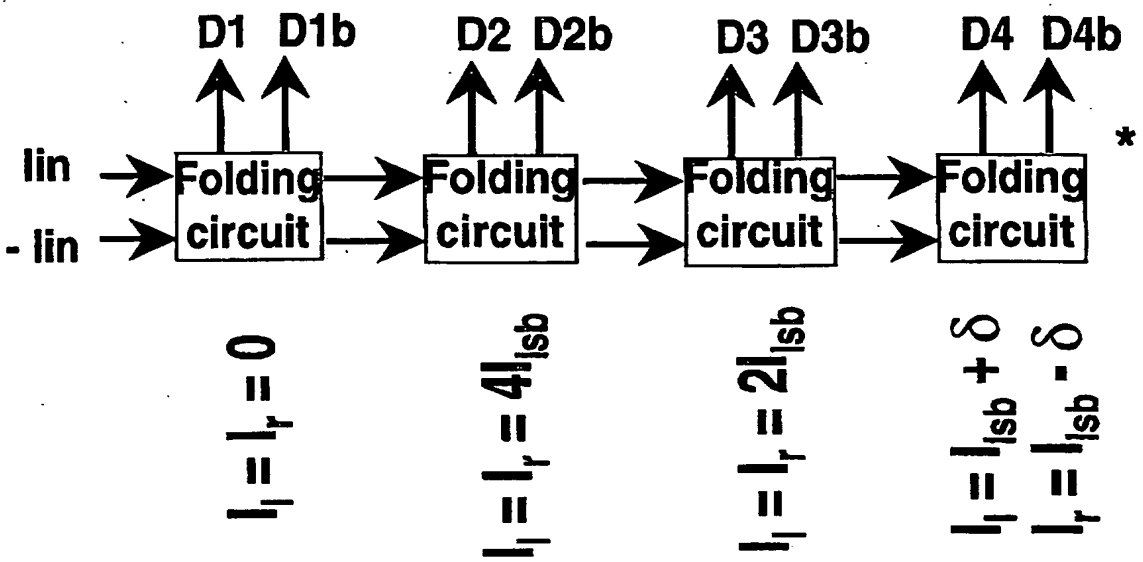
D1 D1b
D2 D2b
D3 D3b
D4 D4b
Iin
- Iin
Folding circuit
Folding circuit
Folding circuit
Folding circuit
*
$I_l = I_r = 0$
$I_l = I_r = 4I_{lsb}$
$I_l = I_r = 2I_{lsb}$
$I_l = I_{lsb} + \delta$
$I_r = I_{lsb} - \delta$

Fig. 29

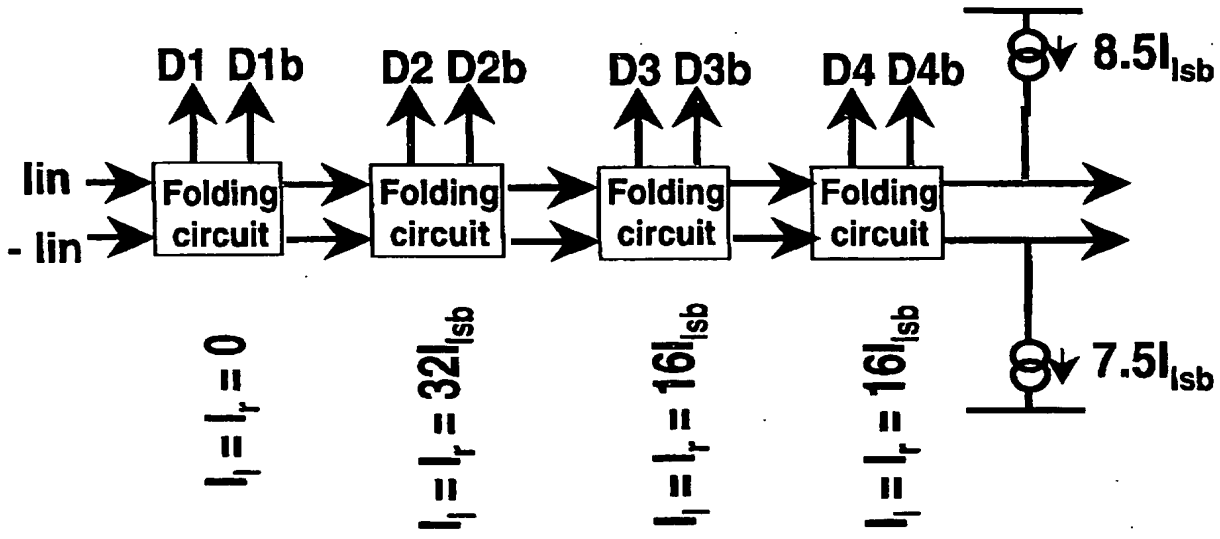
D1 D1b
D2 D2b
D3 D3b
D4 D4b
Iin
- Iin
Folding circuit
Folding circuit
Folding circuit
Folding circuit
$8.5I_{lsb}$
$7.5I_{lsb}$
$I_l = I_r = 0$
$I_l = I_r = 32I_{lsb}$
$I_l = I_r = 16I_{lsb}$
$I_l = I_r = 16I_{lsb}$

Fig. 30

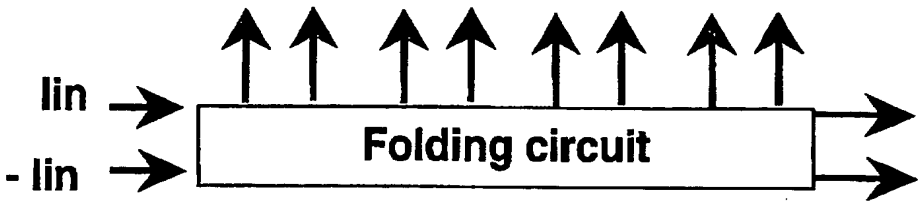
Iin
- Iin
Folding circuit

Fig. 31

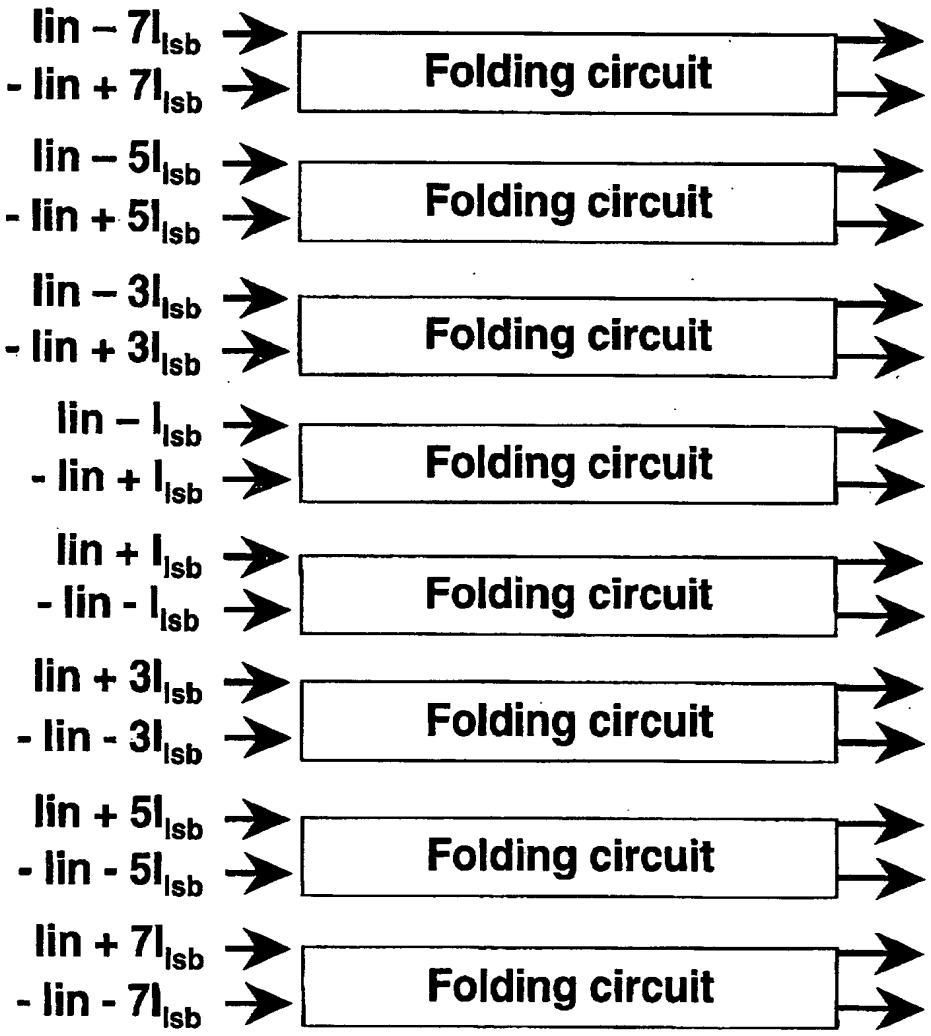
Iin – 7Ilsb
- Iin + 7Ilsb
Folding circuit
Iin – 5Ilsb
- Iin + 5Ilsb
Folding circuit
Iin – 3Ilsb
- Iin + 3Ilsb
Folding circuit
Iin – Ilsb
- Iin + Ilsb
Folding circuit
Iin + Ilsb
- Iin - Ilsb
Folding circuit
Iin + 3Ilsb
- Iin - 3Ilsb
Folding circuit
Iin + 5Ilsb
- Iin - 5Ilsb
Folding circuit
Iin + 7Ilsb
- Iin - 7Ilsb
Folding circuit

Fig. 32

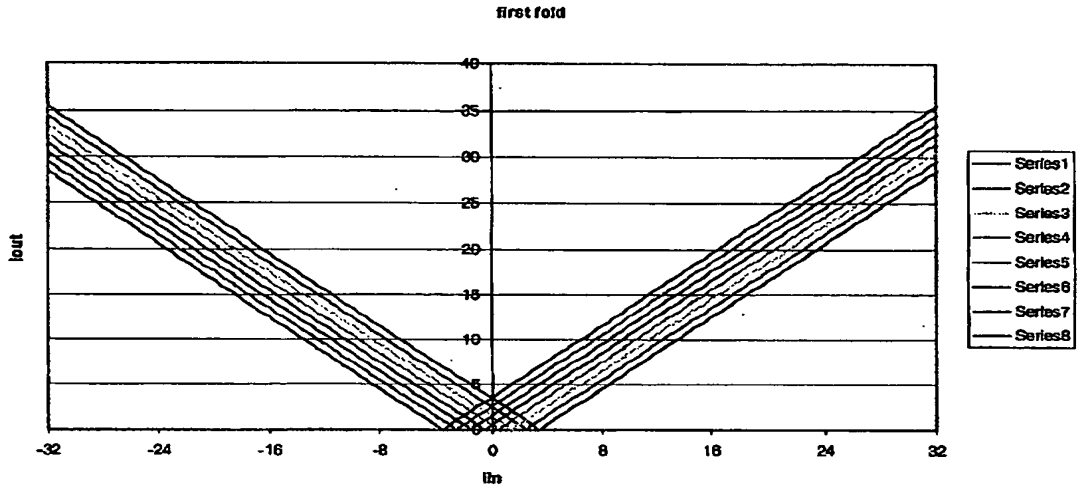
first fold
40
35
30
25
20
15
10
5
0
-32
-24
-16
-8
0
8
16
24
32
Iout
Iin
Series1
Series2
Series3
Series4
Series5
Series6
Series7
Series8

Fig. 33

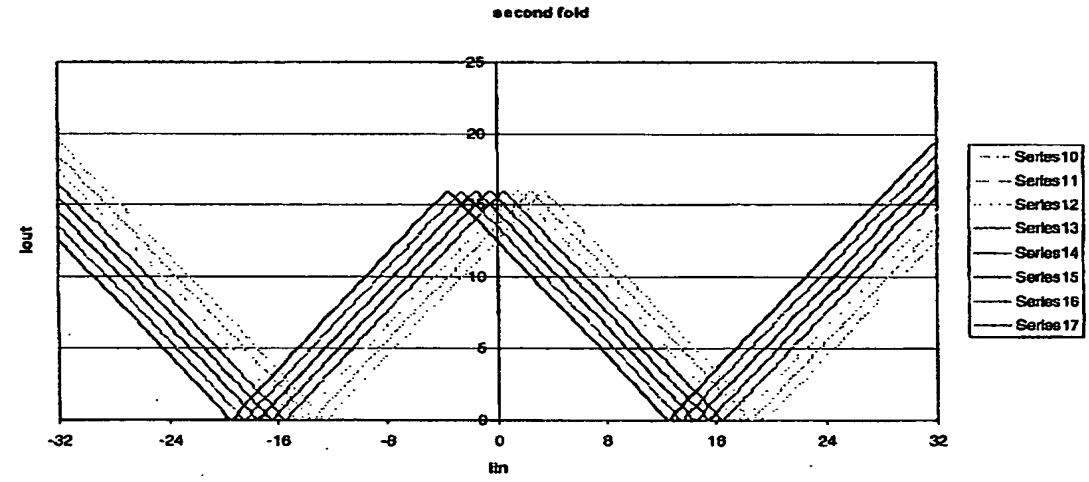
second fold
25
20
15
10
5
0
-32
-24
-16
-8
0
8
16
24
32
Iout
Iin
Series10
Series11
Series12
Series13
Series14
Series15
Series16
Series17

Fig. 34

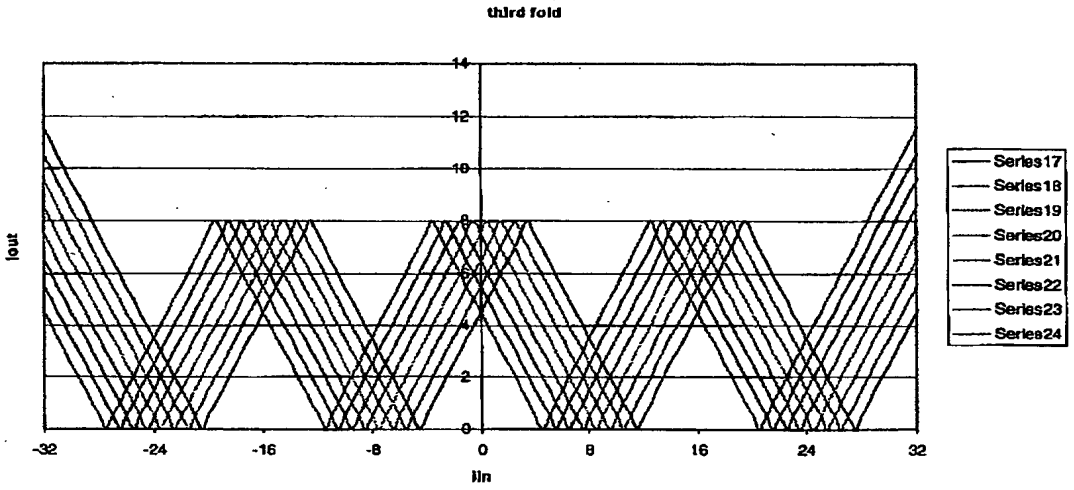
third fold
fout
14
12
10
8
6
4
2
0
-32
-24
-16
-8
0
8
16
24
32
iin
Series17
Series18
Series19
Series20
Series21
Series22
Series23
Series24

Fig. 35

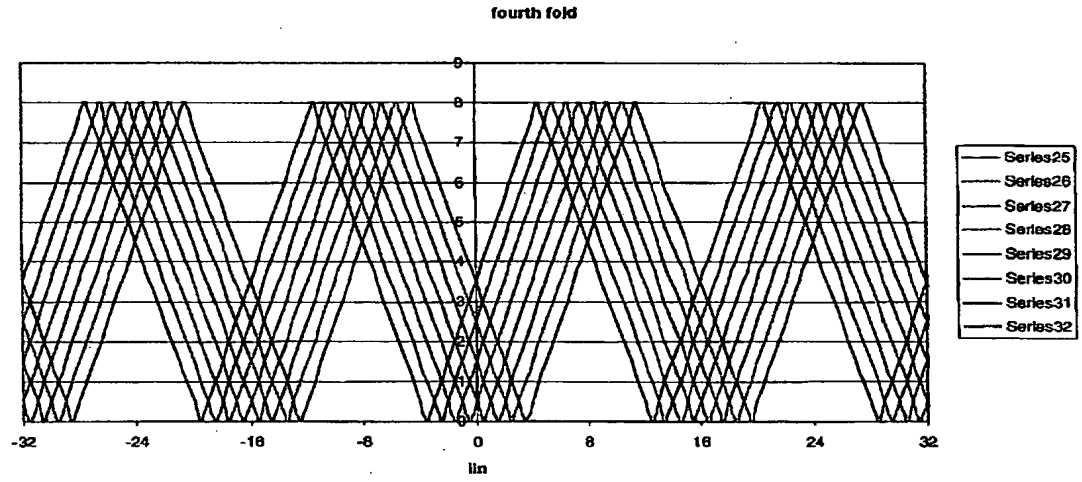
fourth fold
9
8
7
6
5
4
3
2
1
0
-32
-24
-16
-8
0
8
16
24
32
iin
Series25
Series26
Series27
Series28
Series29
Series30
Series31
Series32

Fig. 36

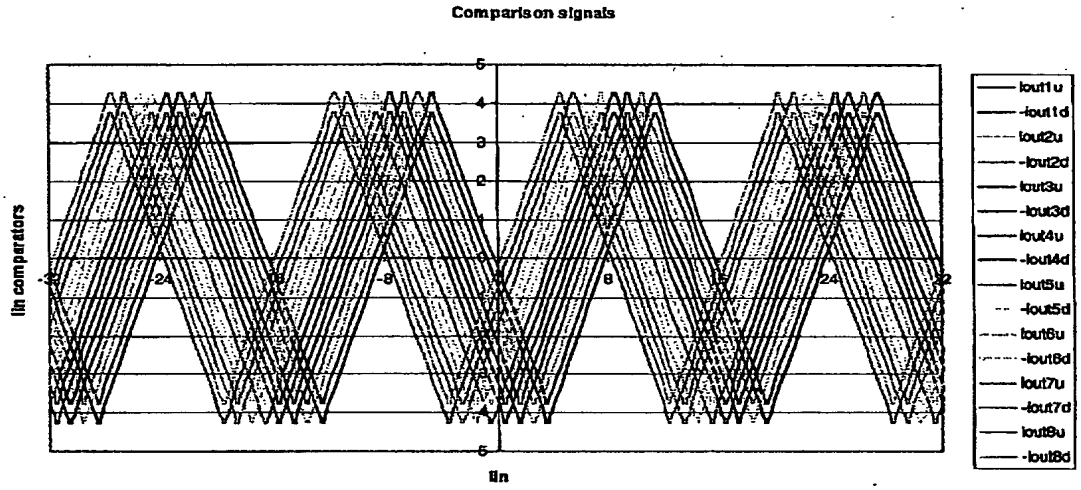
Comparison signals
Iin comparators
Iin
Iout1u
-Iout1d
Iout2u
-Iout2d
Iout3u
-Iout3d
Iout4u
-Iout4d
Iout5u
-Iout5d
Iout6u
-Iout6d
Iout7u
-Iout7d
Iout8u
-Iout8d

Fig. 37

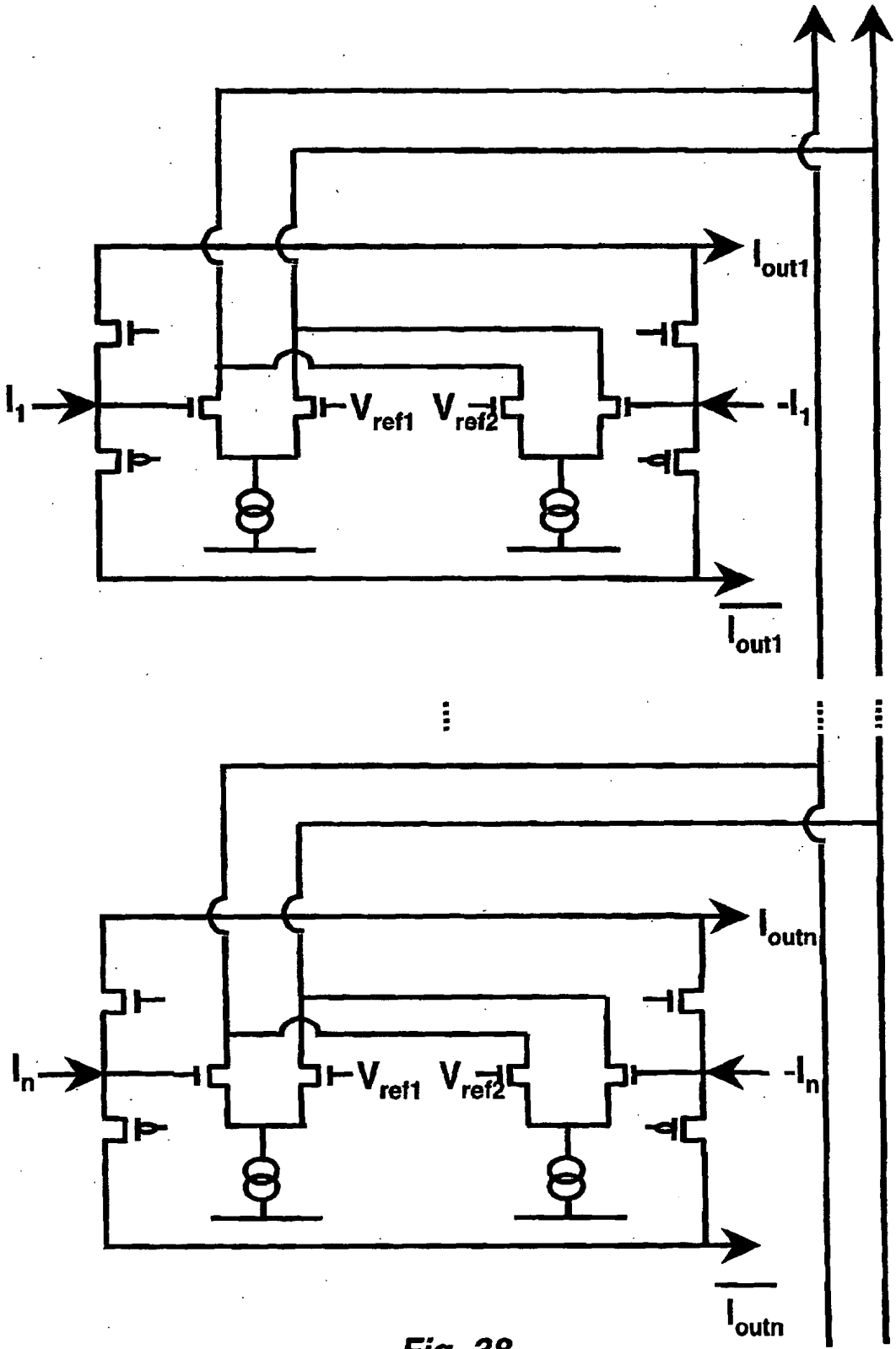
I_{out1}
I_1
V_{ref1}
V_{ref2}
$-I_1$
$\overline{I_{out1}}$
I_{outn}
I_n
V_{ref1}
V_{ref2}
$-I_n$
$\overline{I_{outn}}$

Fig. 38

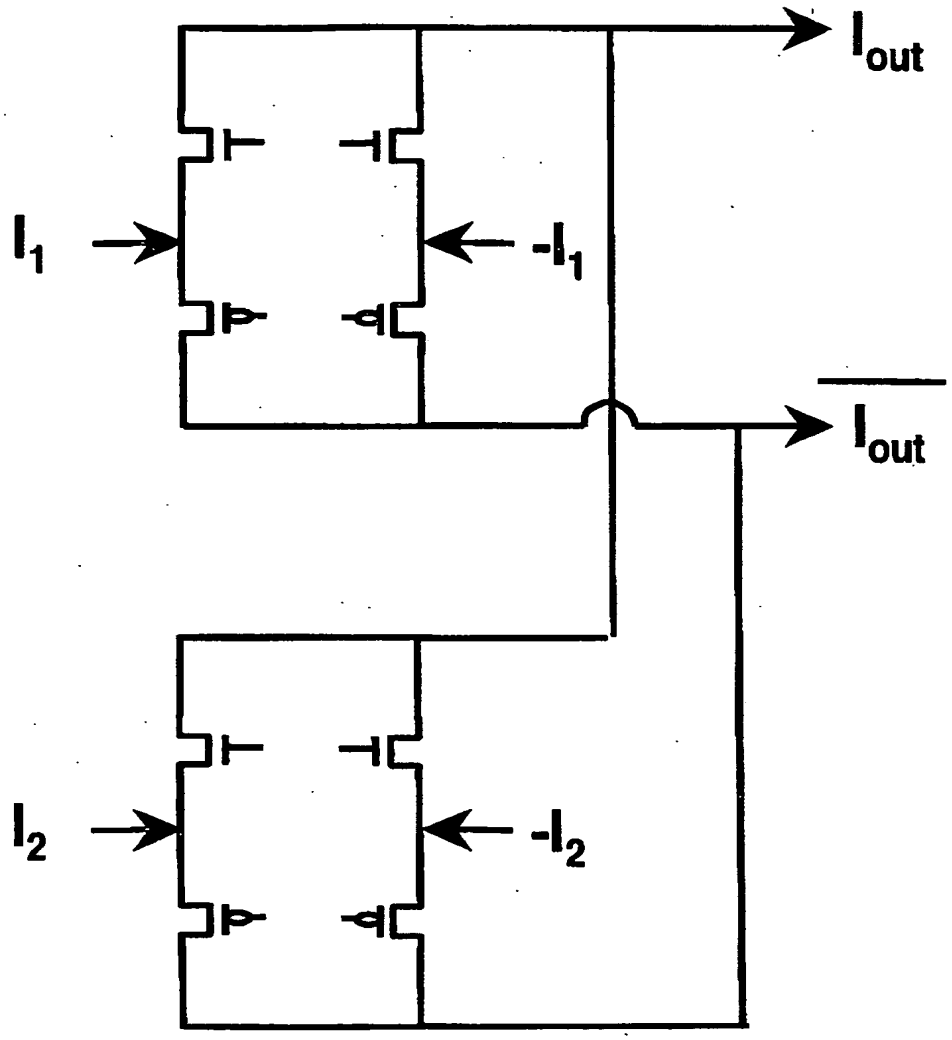

Fig. 39

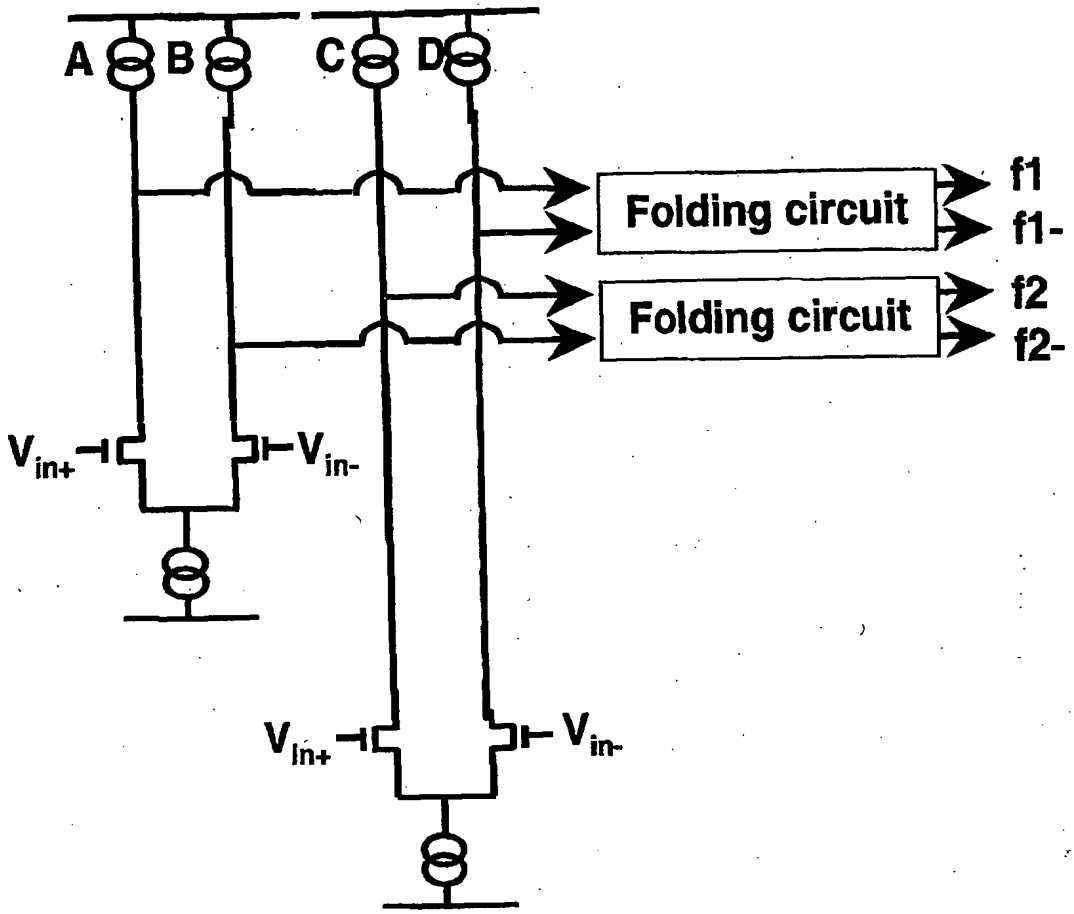
A
B
C
D
Folding circuit
Folding circuit
f1
f1-
f2
f2-
V_{in+}
V_{in-}
V_{in+}
V_{in-}

Fig. 40

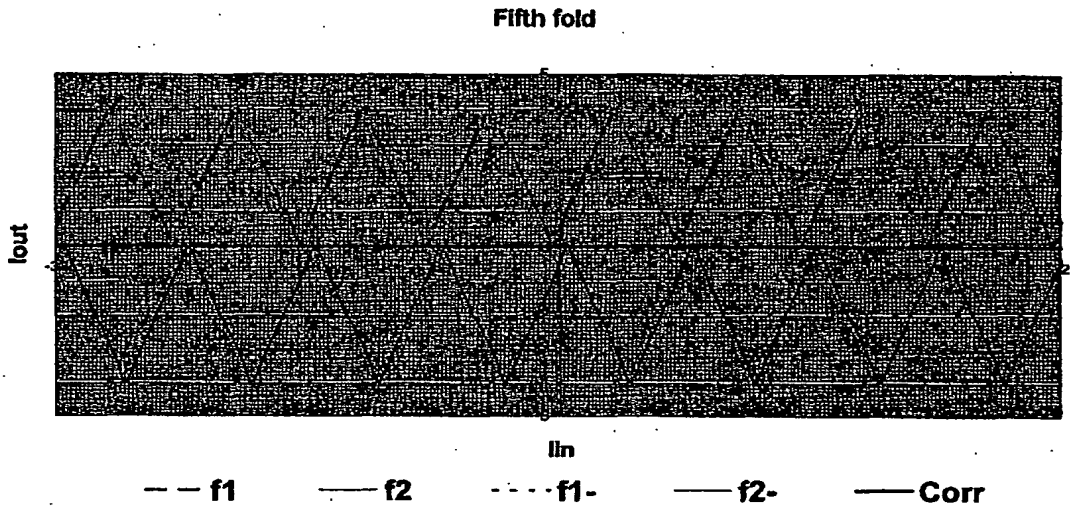
Fifth fold
Iout
Iin
f1
f2
f1-
f2-
Corr

Fig. 41

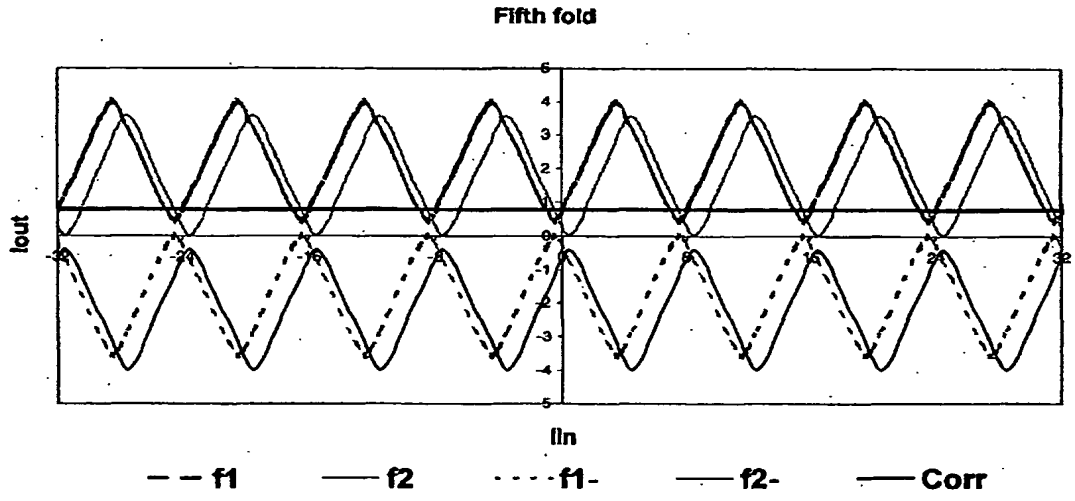
Fifth fold
Iout
Iin
f1
f2
f1-
f2-
Corr

Fig. 42

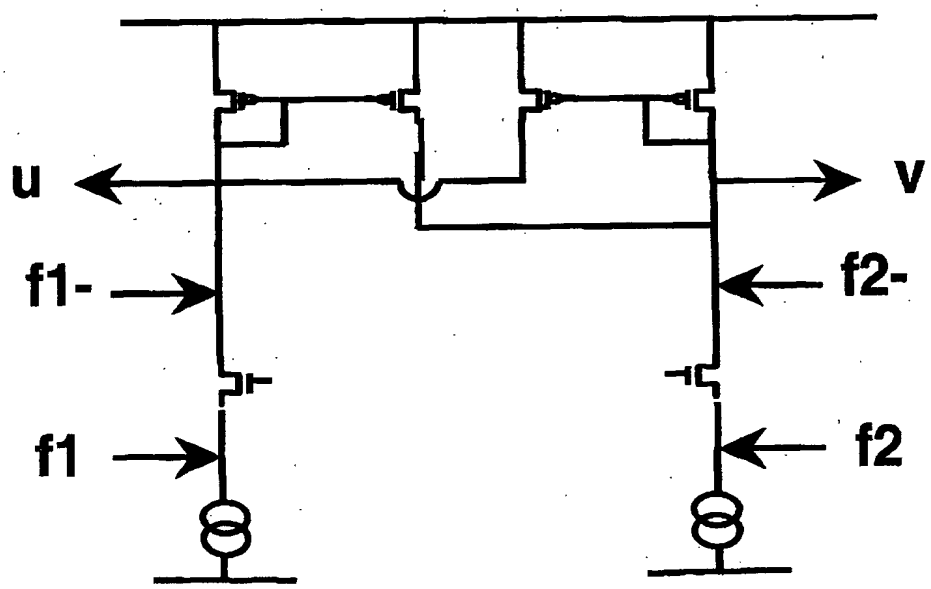

Fig. 43

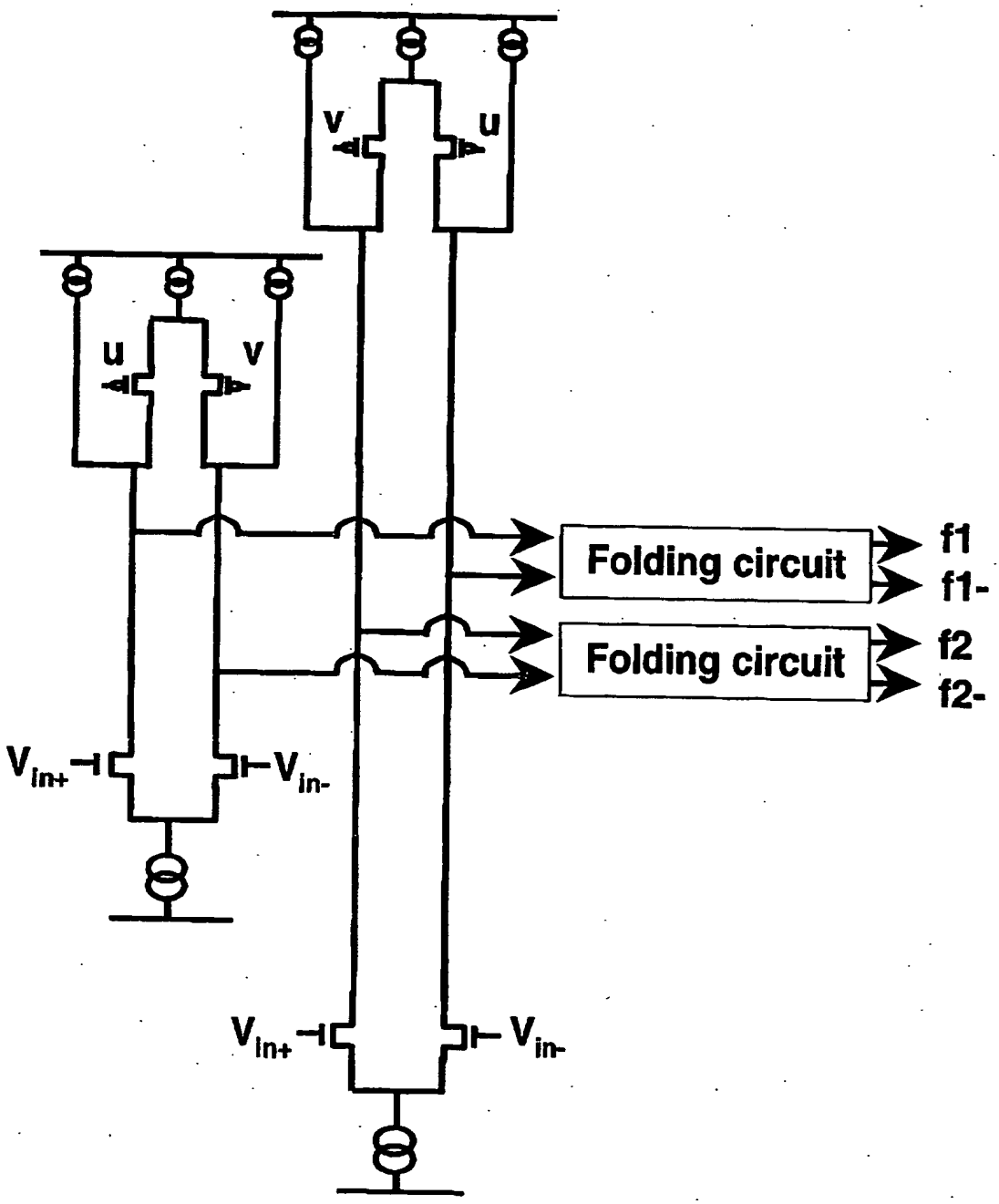
V
U
u
V
Folding circuit
f1
f1-
Folding circuit
f2
f2-
V_{in+}
V_{in-}
V_{in+}
V_{in-}

Fig. 44

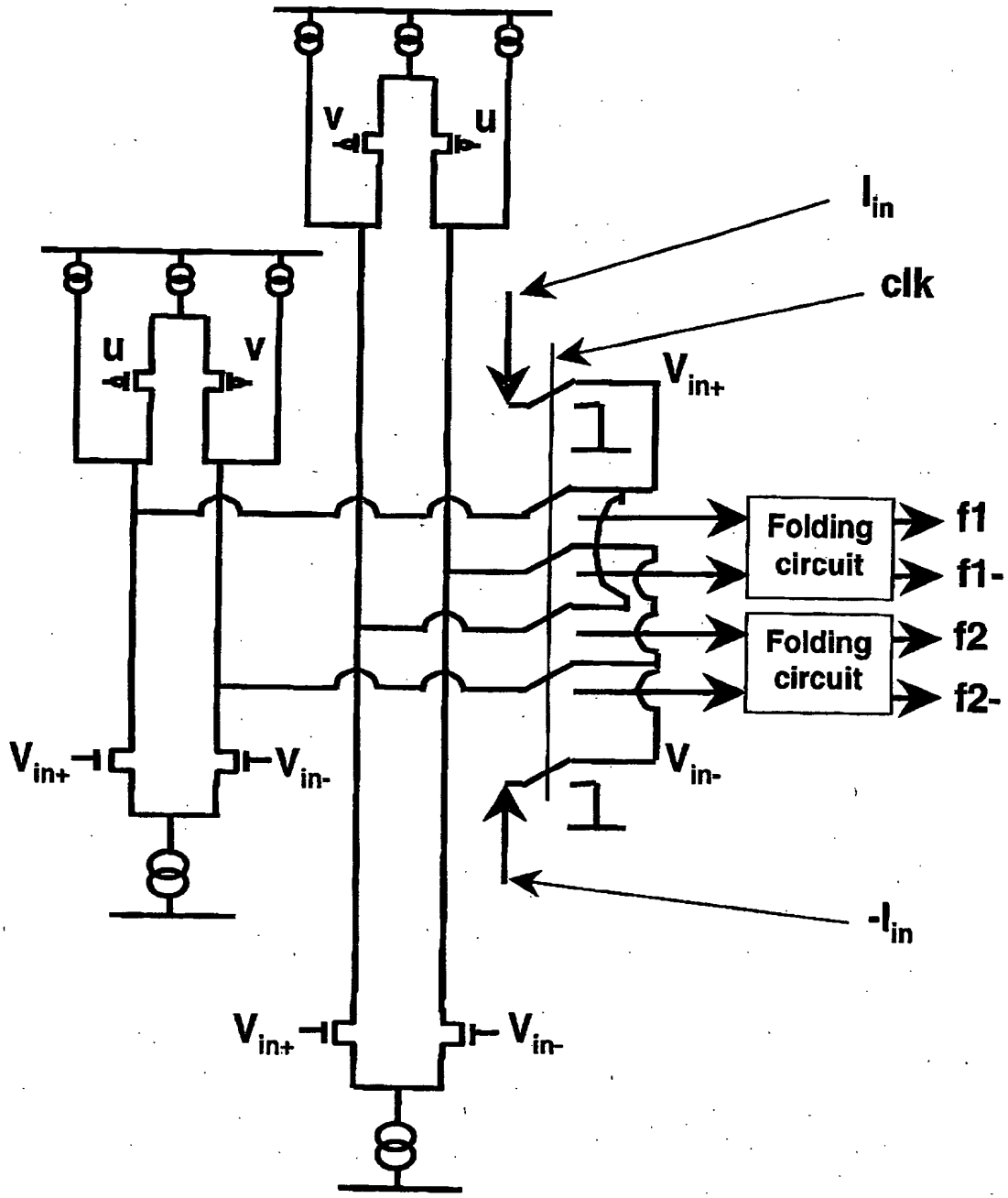
V
u
u
v
I_{in}
clk
V_{in+}
Folding circuit
f1
f1-
Folding circuit
f2
f2-
V_{in+}
V_{in-}
V_{in-}
$-I_{in}$
V_{in+}
V_{in-}

Fig. 45

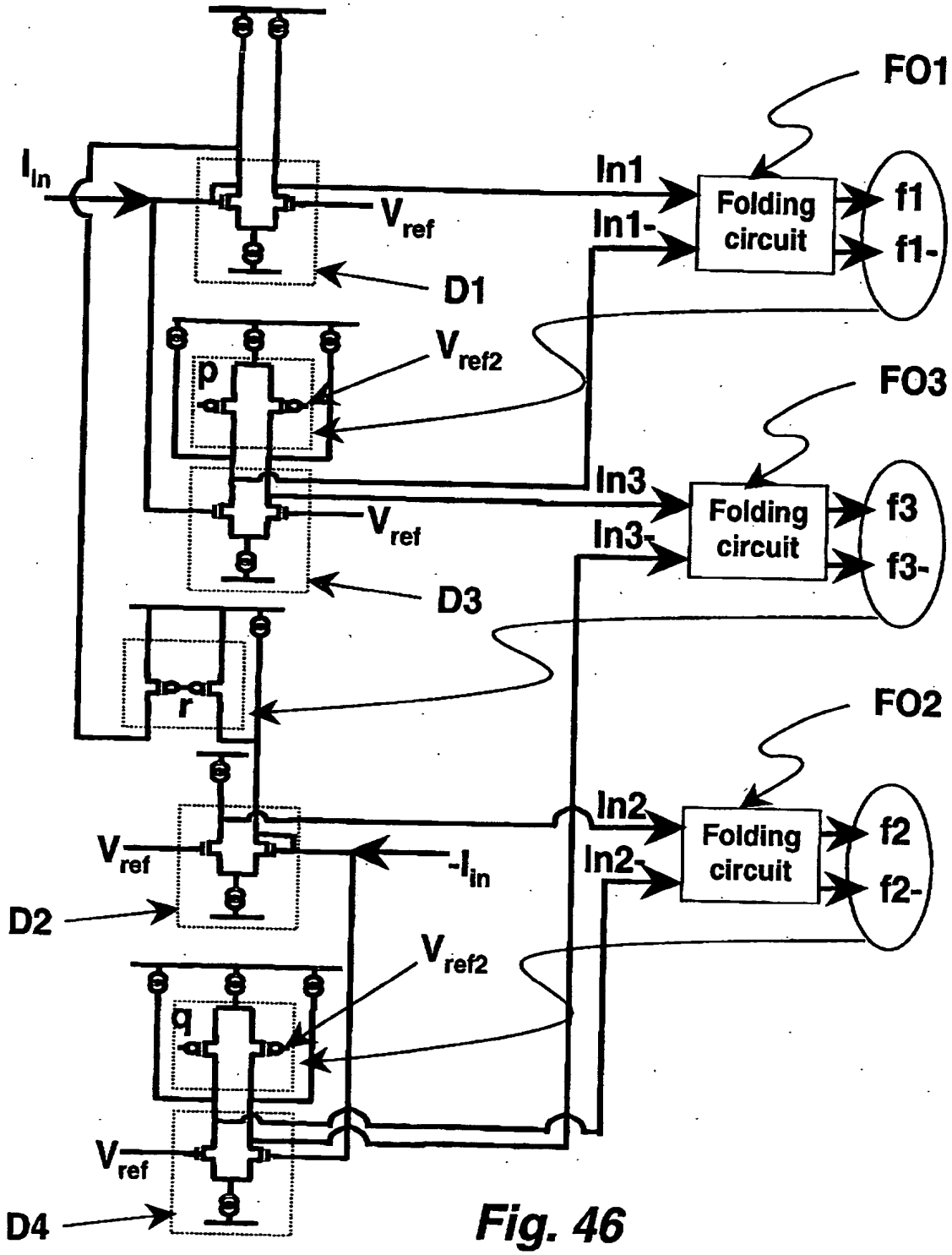
FO1
I_{in}
In1
In1-
V_{ref}
Folding circuit
f1
f1-
D1
V_{ref2}
p
FO3
In3
In3-
V_{ref}
Folding circuit
f3
f3-
D3
r
FO2
In2
In2-
V_{ref}
$-I_{in}$
Folding circuit
f2
f2-
D2
V_{ref2}
q
V_{ref}
D4

Fig. 46

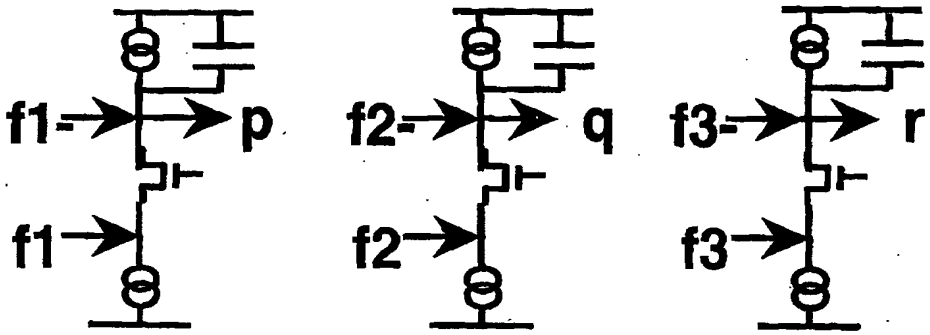

Fig. 47

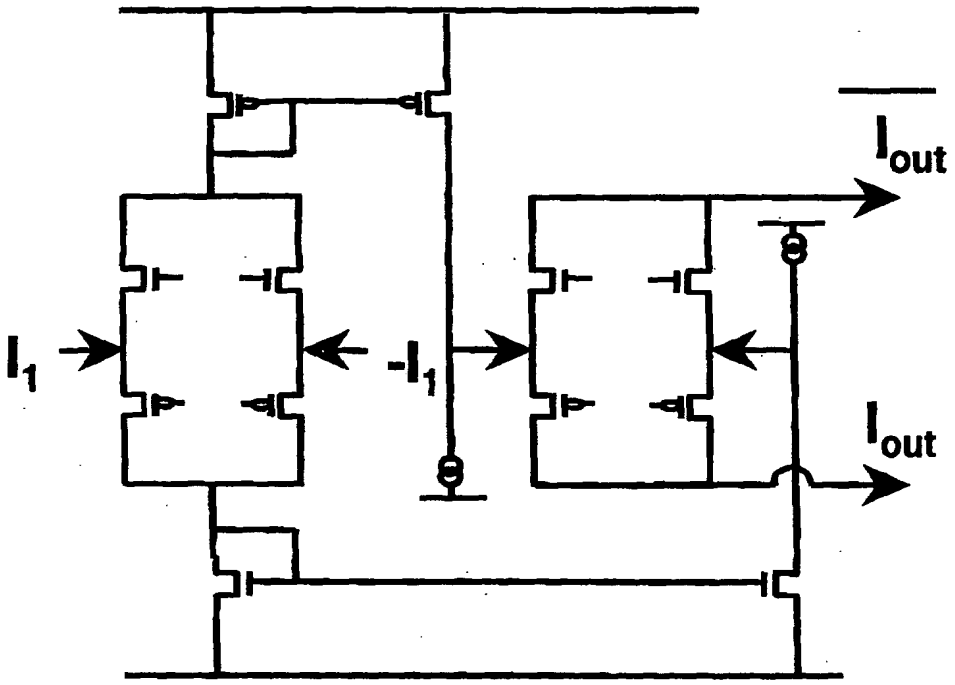

Fig. 48

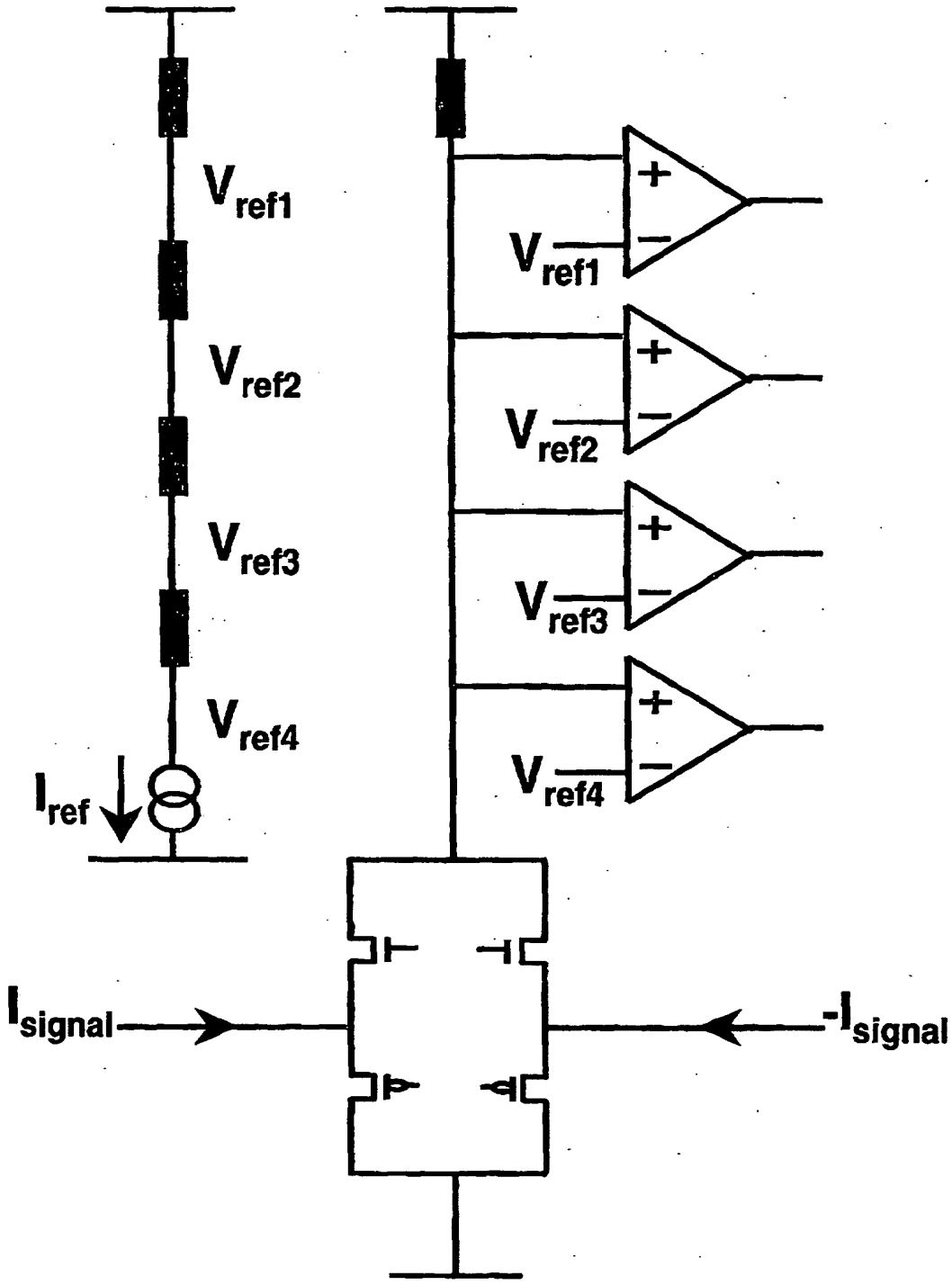
V_{ref1}
V_{ref2}
V_{ref3}
V_{ref4}
I_{ref}
V_{ref1}
V_{ref2}
V_{ref3}
V_{ref4}
I_{signal}
$-I_{signal}$

Fig. 49

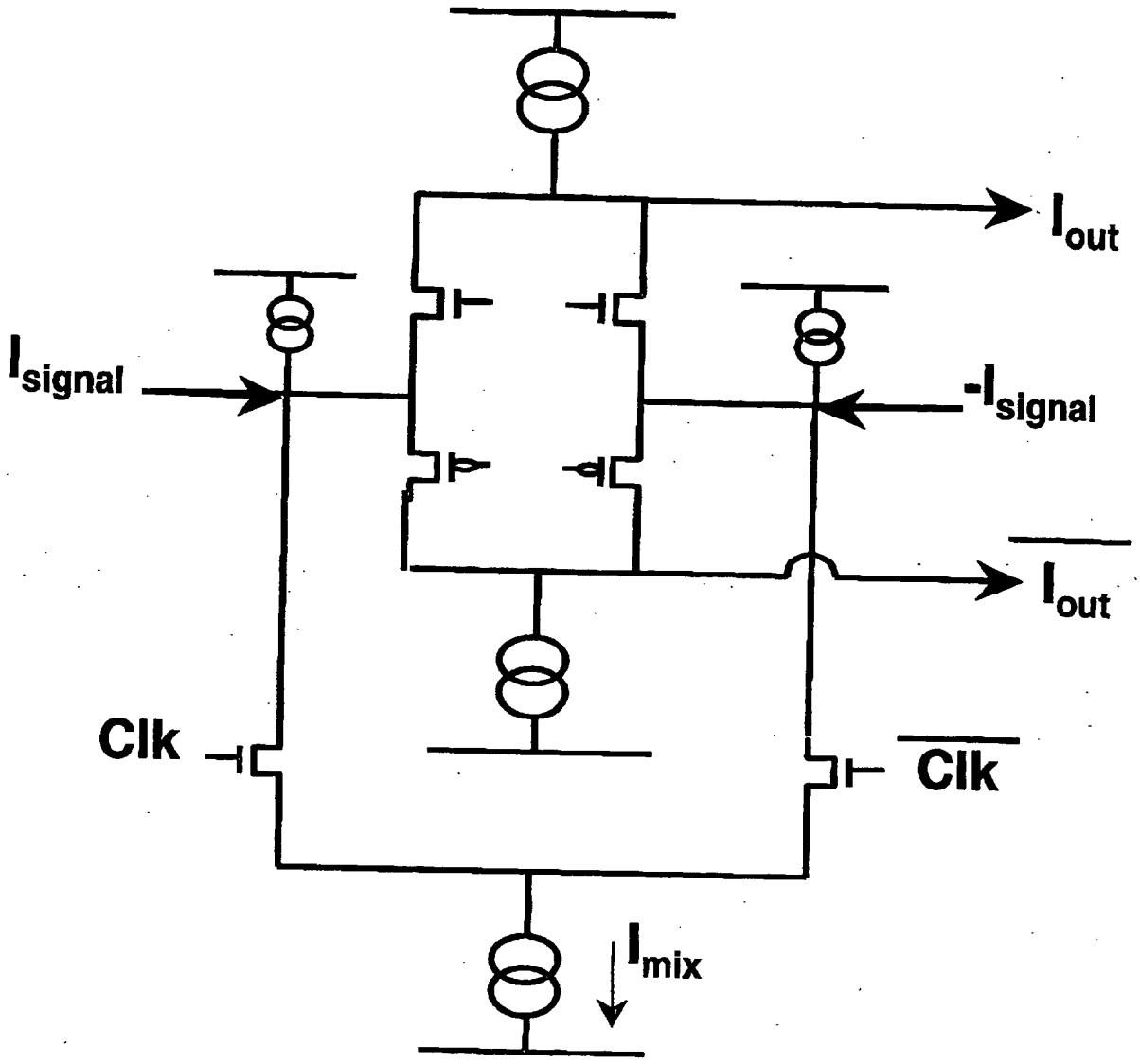

Fig. 50

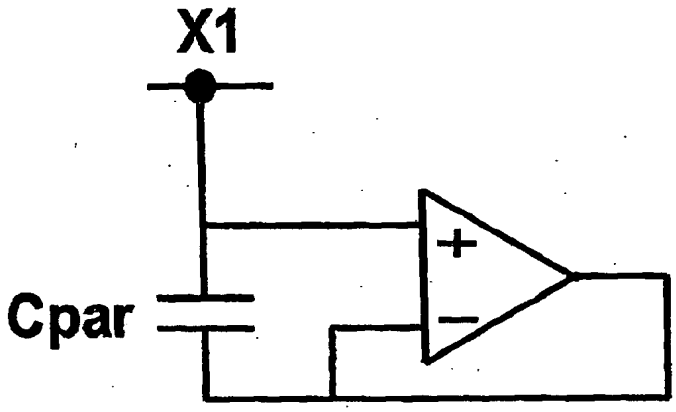

Fig. 51

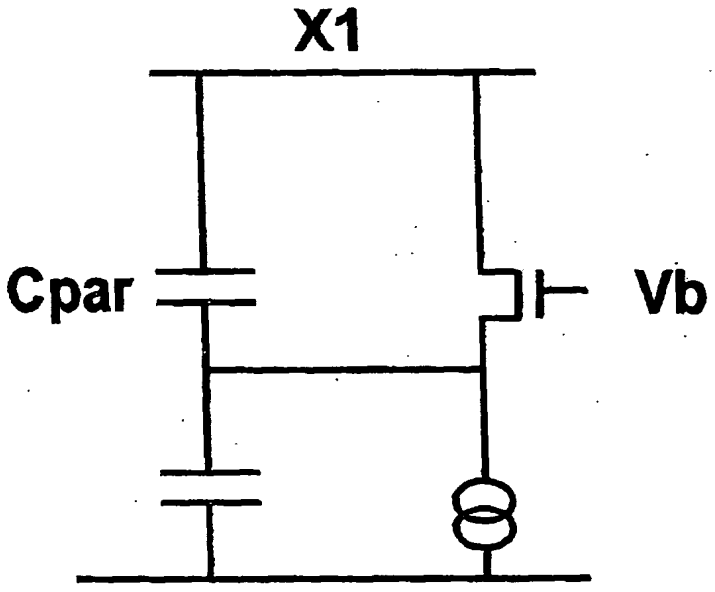

Fig. 52

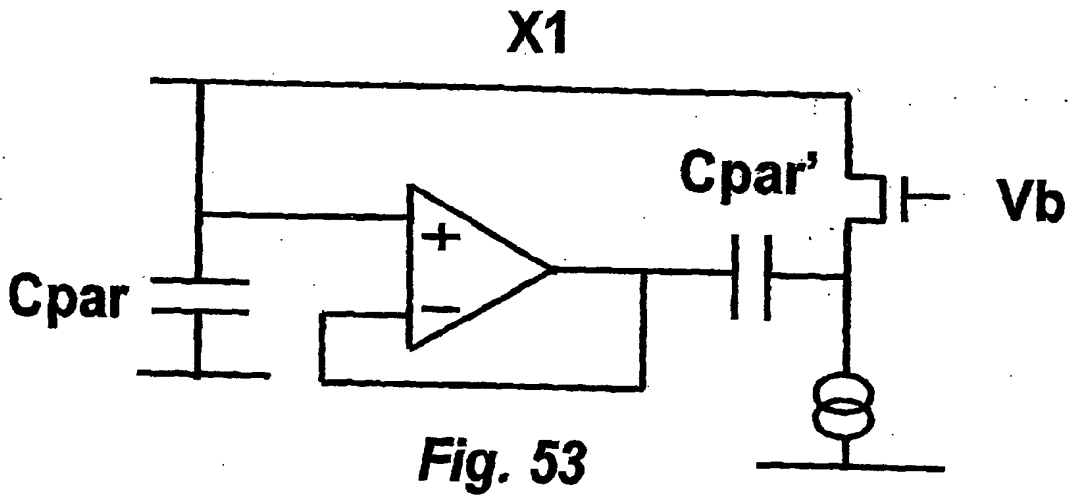

Fig. 53

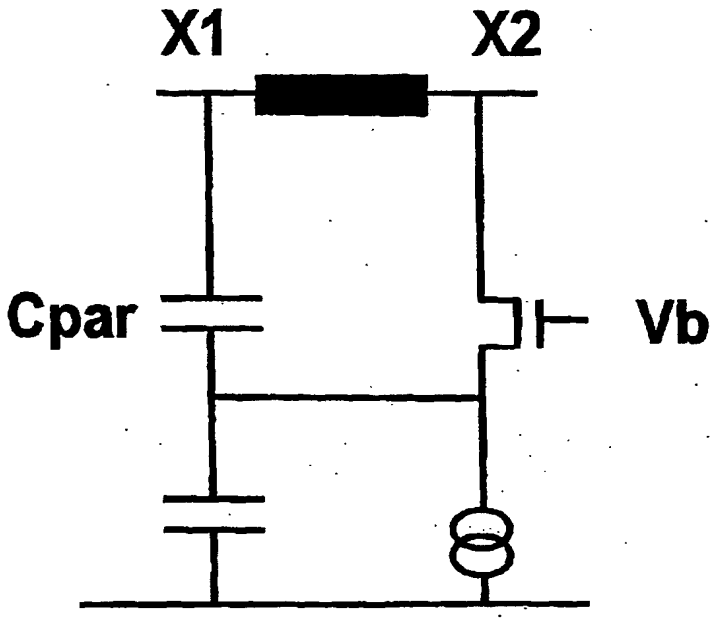

Fig. 54

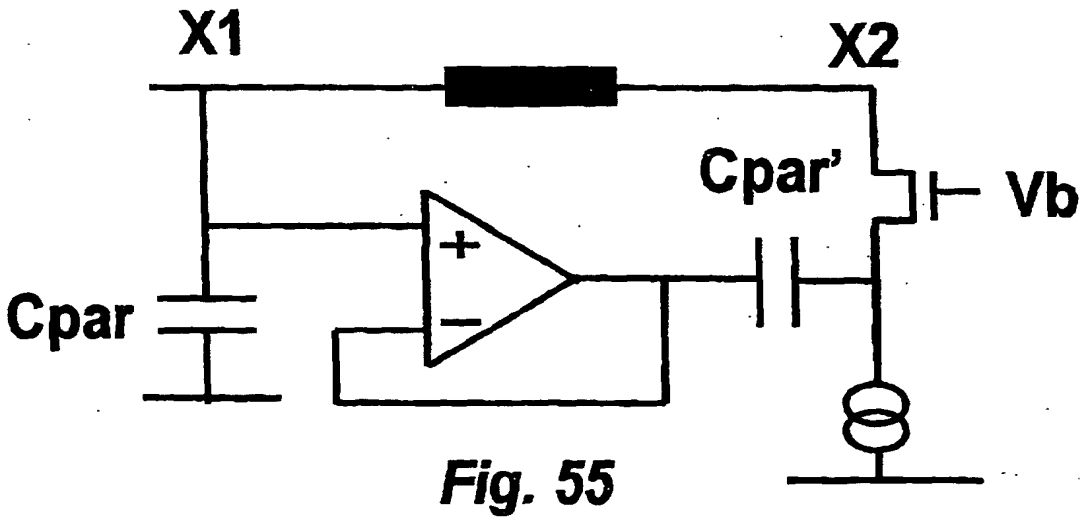

Fig. 55

Abstract

A current folding cell has current inputs and current outputs. Input currents are transferred from one current path to another and finally leading to the current outputs to establish a continuous folding characteristic. The signal current through one of the current paths often does not need to be substantially zero around the folding point in the folding characteristic. Comparator outputs in the cell provide digital outputs corresponding to the currents at the current inputs. An A/D converter can be constructed utilizing such current folding circuit cells in cascade and/or in parallel. The well-determined relationship between folder outputs can be used in a feedback loop to reduce or eliminate mismatch contributions. A mixer can be constructed using such current folding cells.

(Fig. 9)